

COMPAL CONFIDENTIAL

MODEL NAME : ZAR00

PCB NO : LA-B541P

BOM P/N : i5 - 4319TQ31L01 (HSW)
i7 - 4319TQ31L02 (HSW)

GPIO MAP: GPIO map rev 3.6C

Delray 17

Broadwell H-type (2 chip)

REV : 0.1 (X00)

2014.01.13

@ : Nopop Component

EMC@ : EMI/ESD/RF part

CONN@ : Connector Component

PXDP@,CXDP@ : Total debug Component (pop them until ST)

TB@ : Thunderbolt function

BDW@ : HSW_BDW compatibility circuit

Layout Dell logo



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REV: X00
PWB: XXXXX
DATE: 1403-06

PCB 178 LA-B541P REV0 M8

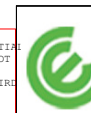
Part Number	Description
DAA0008R000	PCB 178 LA-B541P REV0 M8

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Cover Sheet			
Title	LA-B541P		
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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State	+PWR_SRC +PWR_SRC_S +5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +1.5V_RUN +0.675V_DDR_VTT +VCC_CORE +1.05V_RUN +3.3V_MXM +5V_MXM +MXM_PWR_SRC	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

Stack up

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil
			SolderMask	IT-158
			Add Plating	
1	Top	3.7	Copper foil	0.5oz
2	GND1	3.7	Prepreg	1080
		3.7	Copper foil	1oz
		3.7	Core	4mil
3	Sig 1	3.9	Copper foil	1oz
		3.9	Prepreg	1080H+2116H
4	GND/PWR	3.7	Copper foil	2oz
		3.7	Core	4mil
5	Sig 2	3.8	Copper foil	1oz
		3.8	Prepreg	1080Hb2
6	Sig 3	3.7	Copper foil	1oz
		3.7	Core	4mil
7	GND/PWR	3.9	Copper foil	2oz
		3.9	Prepreg	1080H+2116H
8	Sig 4	3.7	Copper foil	1oz
		3.7	Core	4mil
9	GND 3	3.7	Copper foil	1oz
		3.7	Prepreg	1080
10	Bottom		Copper foil	0.5oz
			Add Plating	
			SolderMask	57.09
Overall Thickness (1.45mm ± 10%)				

USB3.0	DESTINATION
Port 1	IO Board- JUSB3
Port 2	JUSB1 (Ext Right Side)
Port 3	Docking
Port 4	NA
Port 5	IO Board- JUSB1
Port 6	IO Board- JUSB2

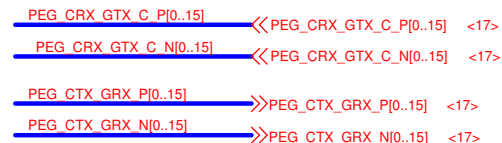
PCH	USB PORT#	DESTINATION
	0	IO Board- JUSB3 (Ext Left Side)
	1	JUSB1 (Ext Right Side)
	2	IO Board- JUSB1 (Ext Left Side)
	3	Docking USB3.0
	4	M.2 Slot-1 (WLAN/BT/WiGig)
	5	M.2 Slot-2 (WWAN/LTE/HCA)
	6	Docking USB 2.0
	7	USH
	8	Camera
	9	IO Board- JUSB2 (Ext Left Side)
	10	M.2 Slot-3 (SSD/HCA/Cache)
	11	Touch Screen
	12	NA
	13	NA
USH	0	BIO
	1	NA

PCI EXPRESS	DESTINATION
Lane 1	M.2 Slot-2 (WWAN/LTE/HCA)
Lane 2	M.2 Slot-3 (SSD/HCA/Cache)
Lane 3	10/100/1G LOM
Lane 4	MMI(Card reader)
Lane 5	TBT-1
Lane 6	TBT-2
Lane 7	M.2 Slot-1 (WLAN/BT/WiGig)
Lane 8	M.2 Slot-1 (WLAN/BT/WiGig)

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Broadwell (1/7)

Size

Document Number

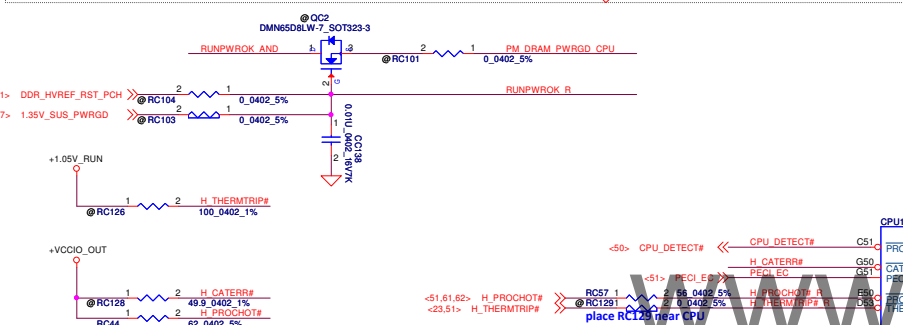
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Rev	0.1
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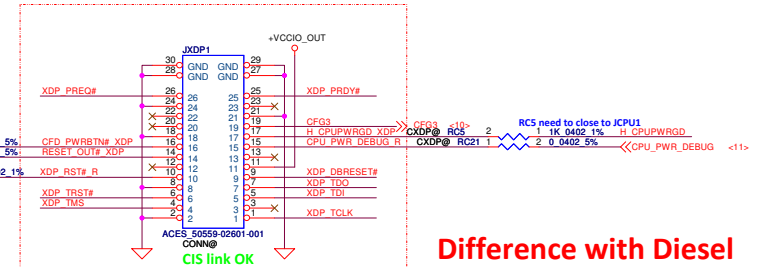
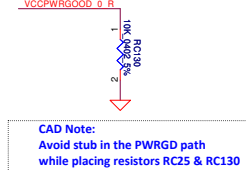
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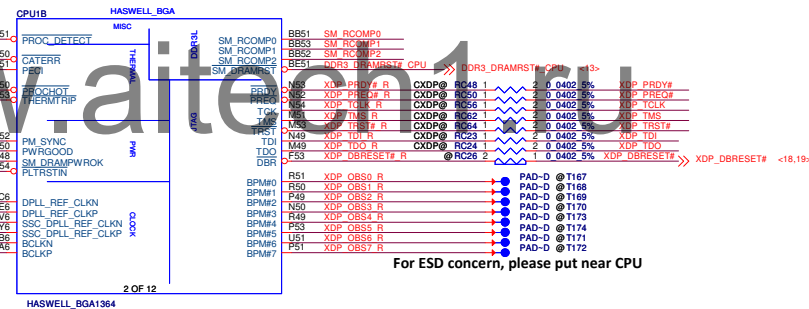
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Remove +1.05V_RUN to +VCCST circuit
for rPGA usage.



2 chip XDP debug component list - CPU side(CXDP@)			
item	Qty	Part reference	Part description
1	1	CC65	SE00000G880 (S CER CAP 0.1U 25V K X5R 0402)
2	9	RC6,RC21,RC48,RC50,RC56,RC62,RC64,RC23,RC24	SD028000080 (S RES 1/16W 0 + -5% 0402)
3	2	RC8,RC5	SD028100180 (S RES 1/16W 1K + -5% 0402)
4	1	JXDP1	LTCX004MX00(ACES 50559-02601-001 26P-T)



3.3V RUN

XDP DBRESET# R RC19 2 1 1K 0402 1%

+1.05V RUN

XDP TMS R @ RC27 2 1 51 0402 1%

XDP TDI R @ RC29 2 1 51 0402 1%

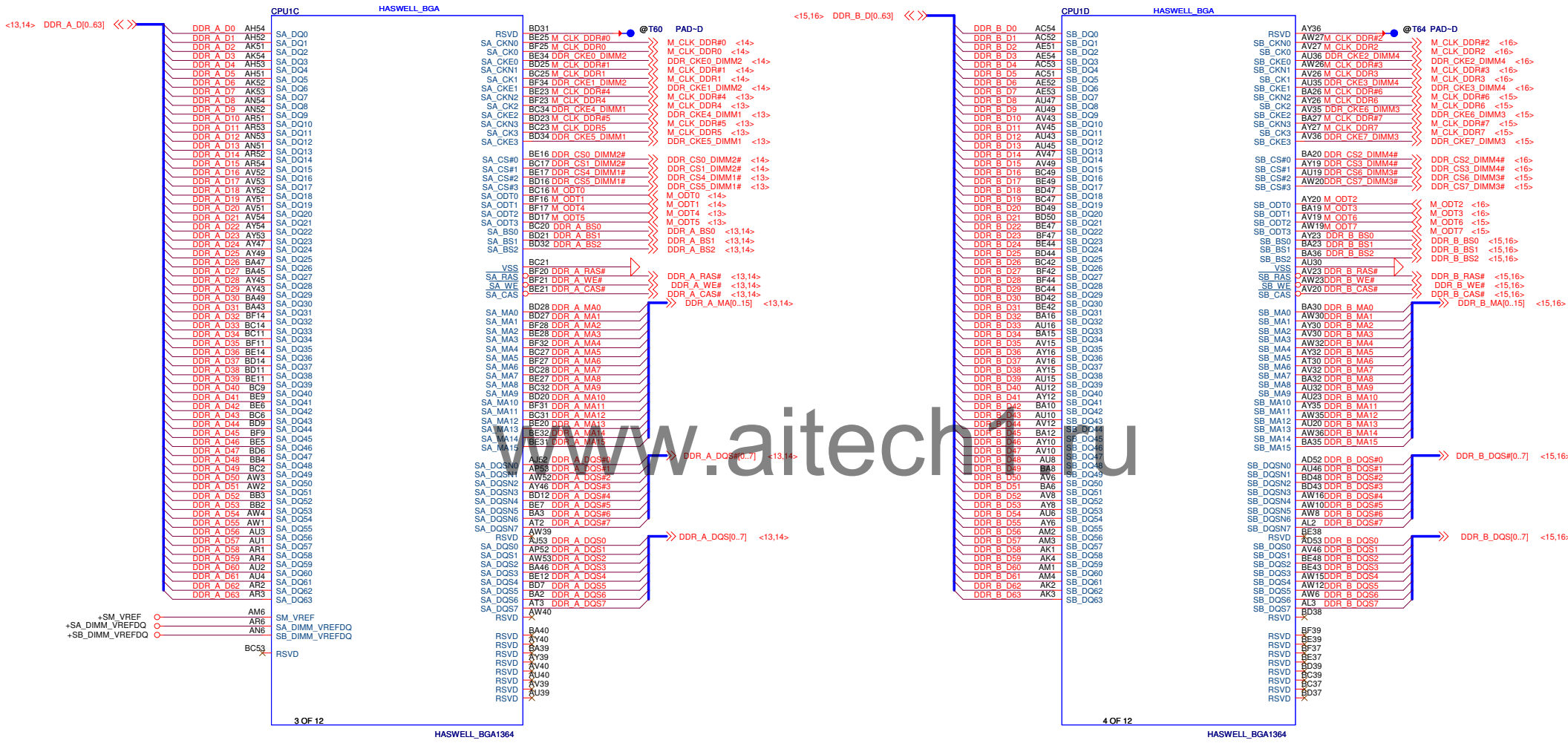
XDP PREQ# R @ RC32 2 1 51 0402 1%

XDP TDO R RC35 2 1 51 0402 1%

XDP TCLK R RC40 2 1 51 0402 1%

XDP TRST# R RC41 2 1 51 0402 1%

CAD Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mil



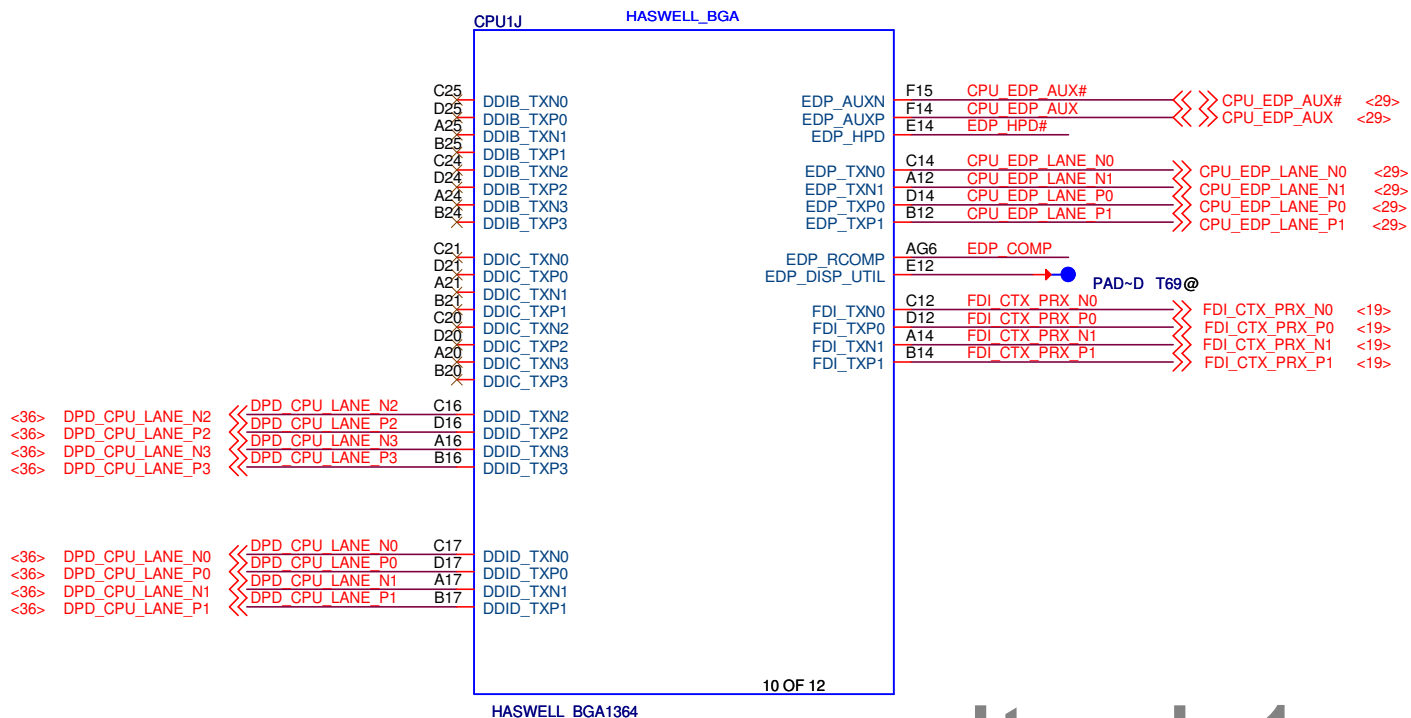
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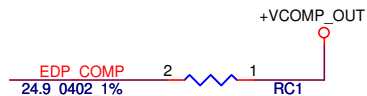
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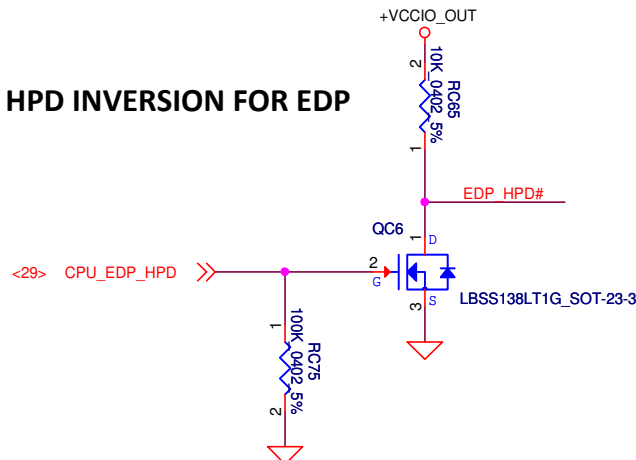
www.aitech1.ru

COMPENSATION PU FOR eDP



CAD Note: Trace width=20 mils ,Spacing=25mil,
Max length=100 mils.

HPD INVERSION FOR EDP



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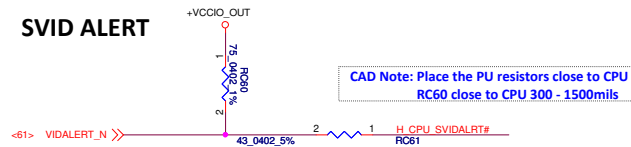
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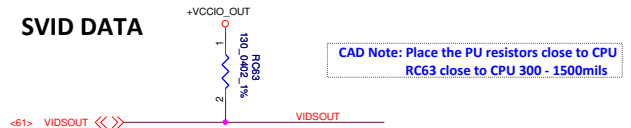
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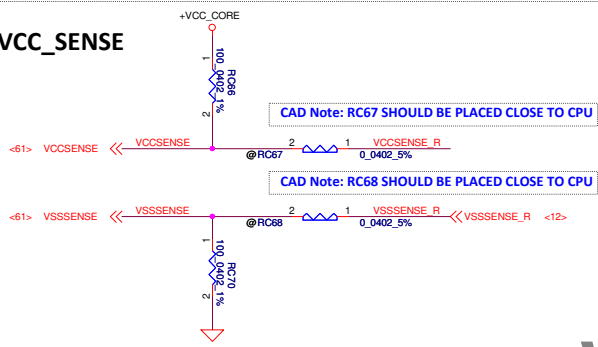
SVID ALERT



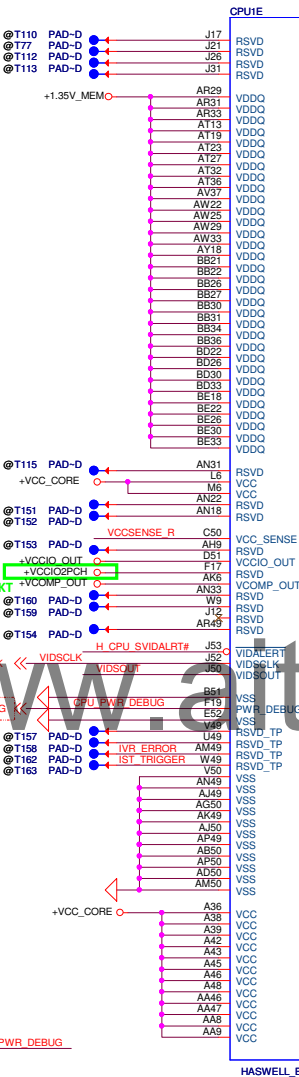
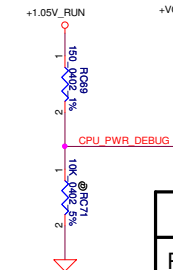
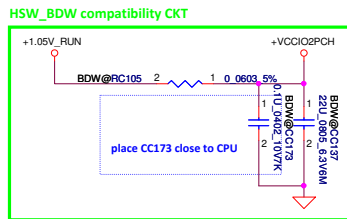
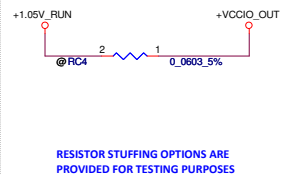
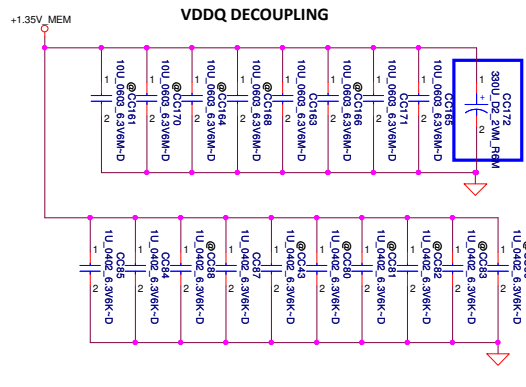
SVID DATA



VCC_SENSE

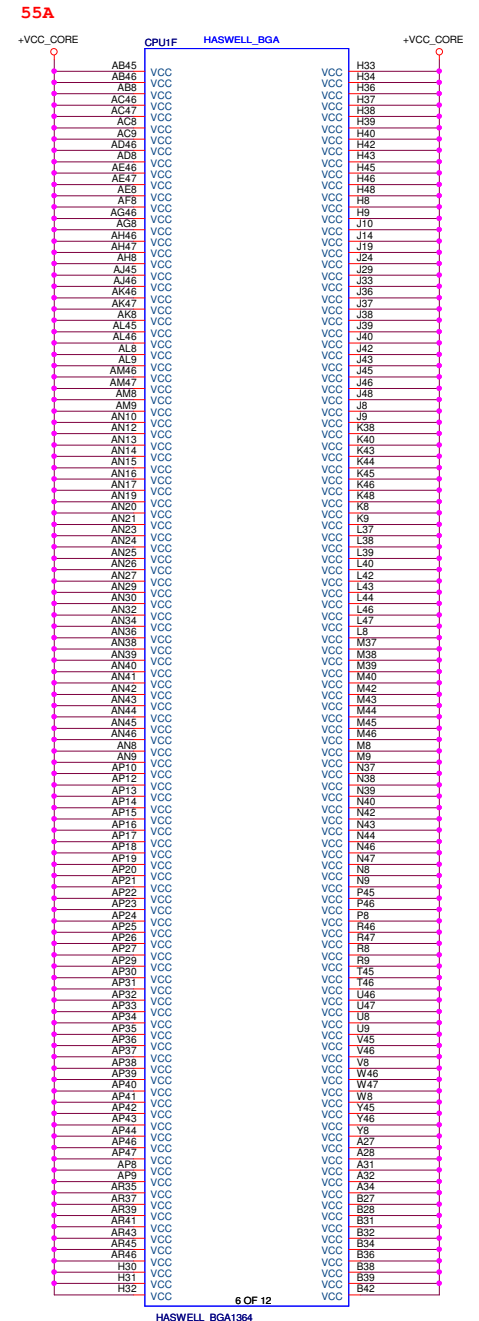
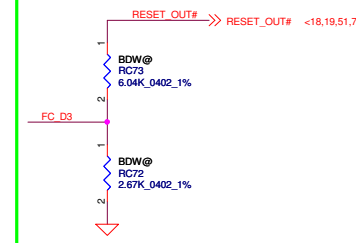


Difference with Diesel (follow HSW-BGA CRB Rev 0.7)



	HSW	BDW
RC105	X	V
CC137	X	V
CC173	X	V
RC72	X	V
RC73	X	V

HSW_BDW compatibility CKT



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Broadwell (6/7)

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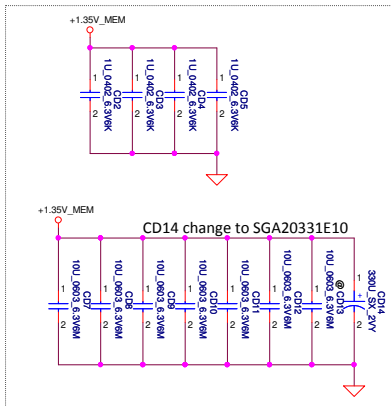
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All VREF traces should have 10 mil trace width

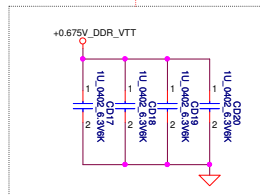
Populate RD1, De-Populate RD2 for Intel DDR3
VREFDQ multiple methods M1
Populate RD2, De-Populate RD1 for Intel DDR3
VREFDQ multiple methods M3

JDIMM1 STD Type H=9.2

<14,8> DDR_A_DQS#0.7] <<>
<14,8> DDR_A_DQS#0.7] <<>
<14,8> DDR_A_DQS#0.7] <<>
<14,8> DDR_A_MA0.15] <<>

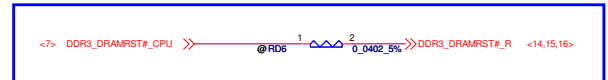
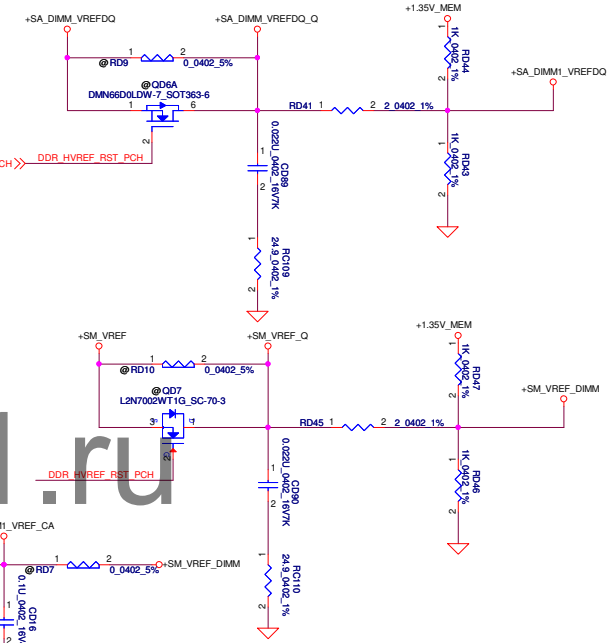
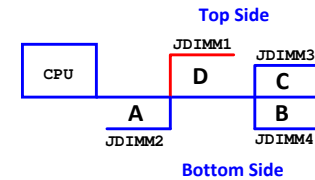
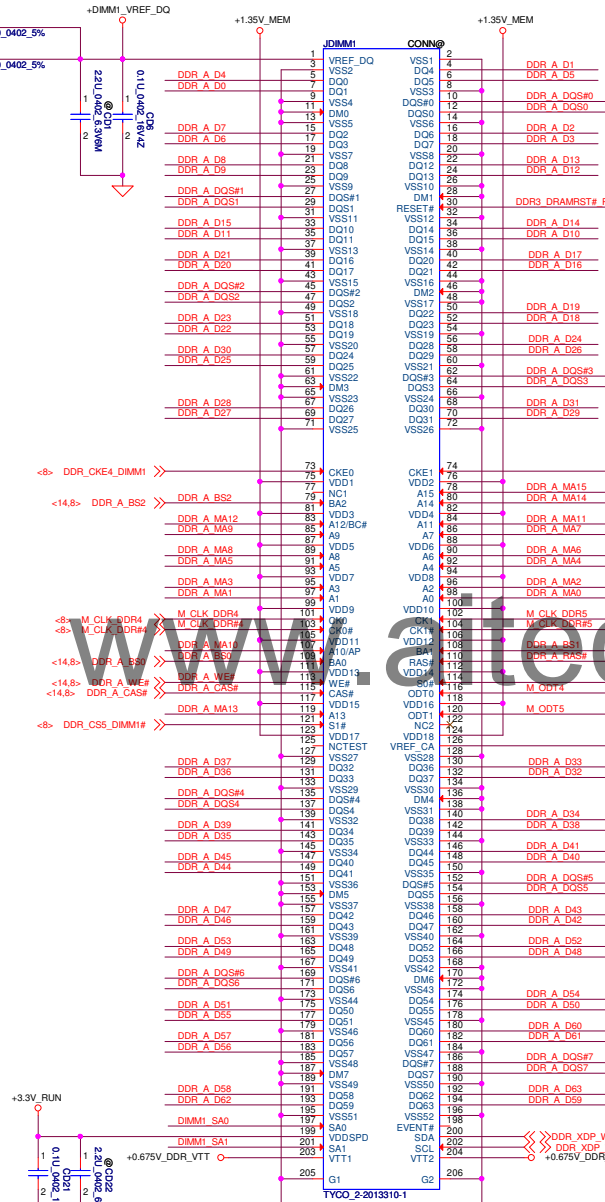


Layout Note:
Place near JDIMM1.203,204



DIMM Select

	SA0	SA1
DIMM2	0	0
DIMM4	0	1
DIMM1	1	0
DIMM3	1	1



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DDR3-SODIMM SLOT1

LA-B541P

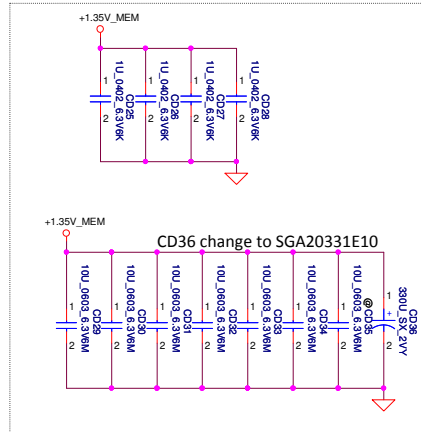
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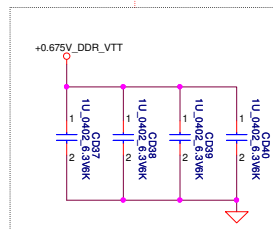
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JDIMM2 STD Type H=5.2

All VREF traces should have 10 mil trace width

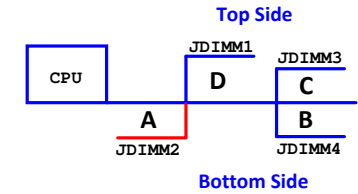
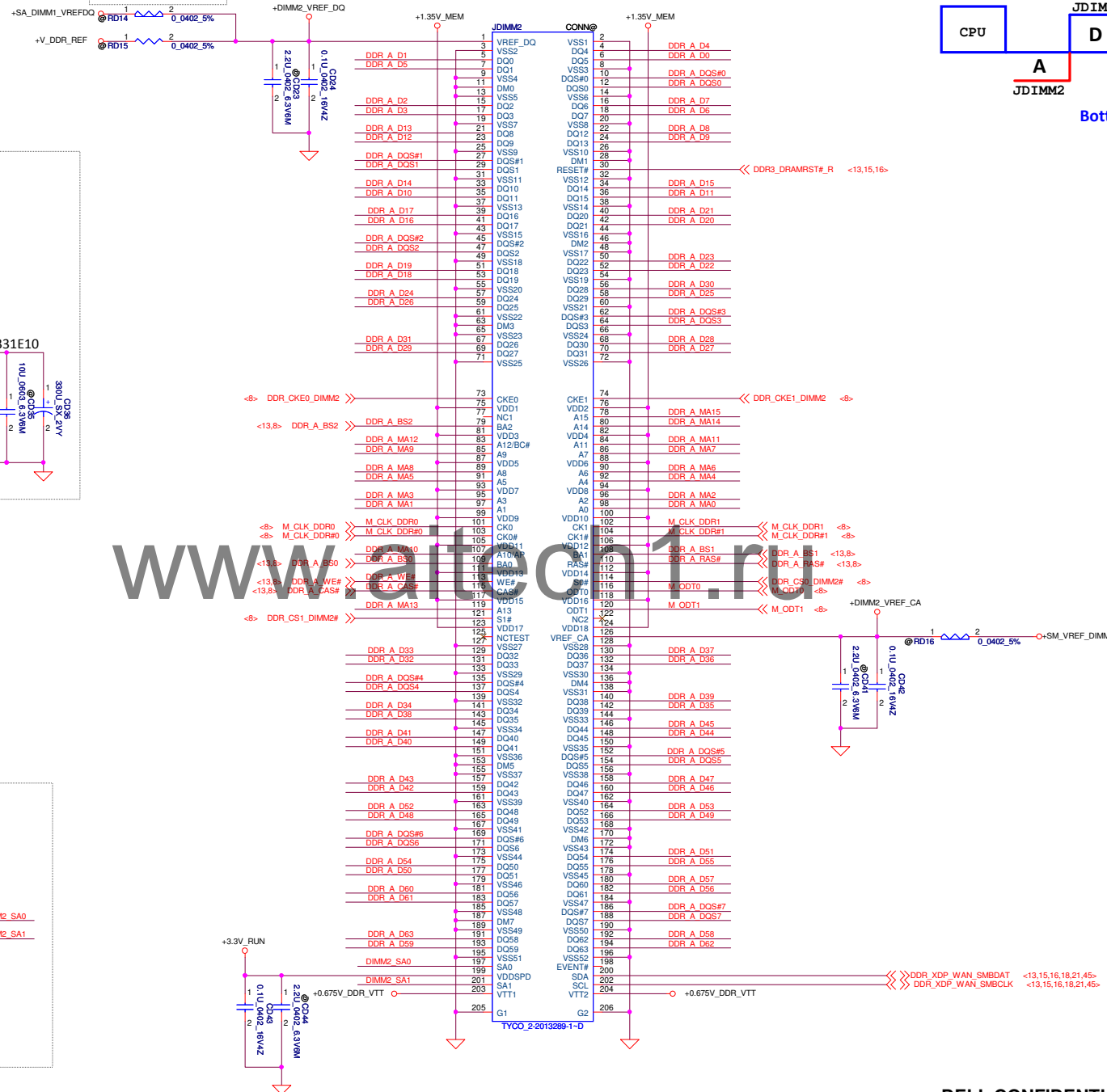
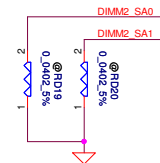


Layout Note:
Place near JDIMM2.Pin 203,204



DIMM Select

	SA0	SA1
DIMM2	0	0
DIMM4	0	1
DIMM1	1	0
DIMM3	1	1



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DDRIII-SODIMM SLOT2

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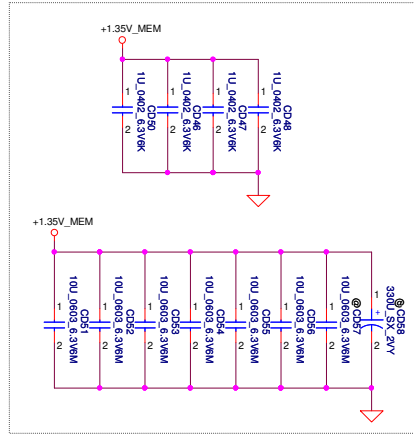
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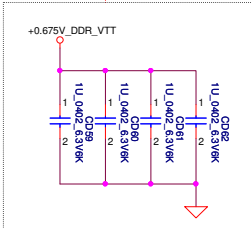
All VREF traces should have 10 mil trace width

JDIMM3 STD Type H=5.2

<16,8> DDR_B_DQS#0[0.7] <>>
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<16,8> DDR_B_DQ[0.63] <>>
<16,8> DDR_B_MA[0.15] <>>

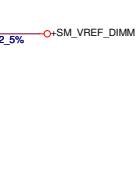
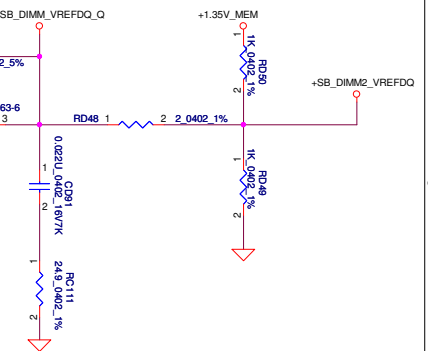
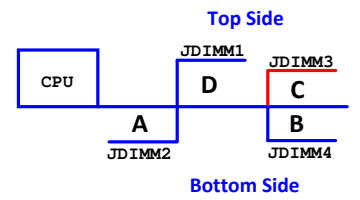
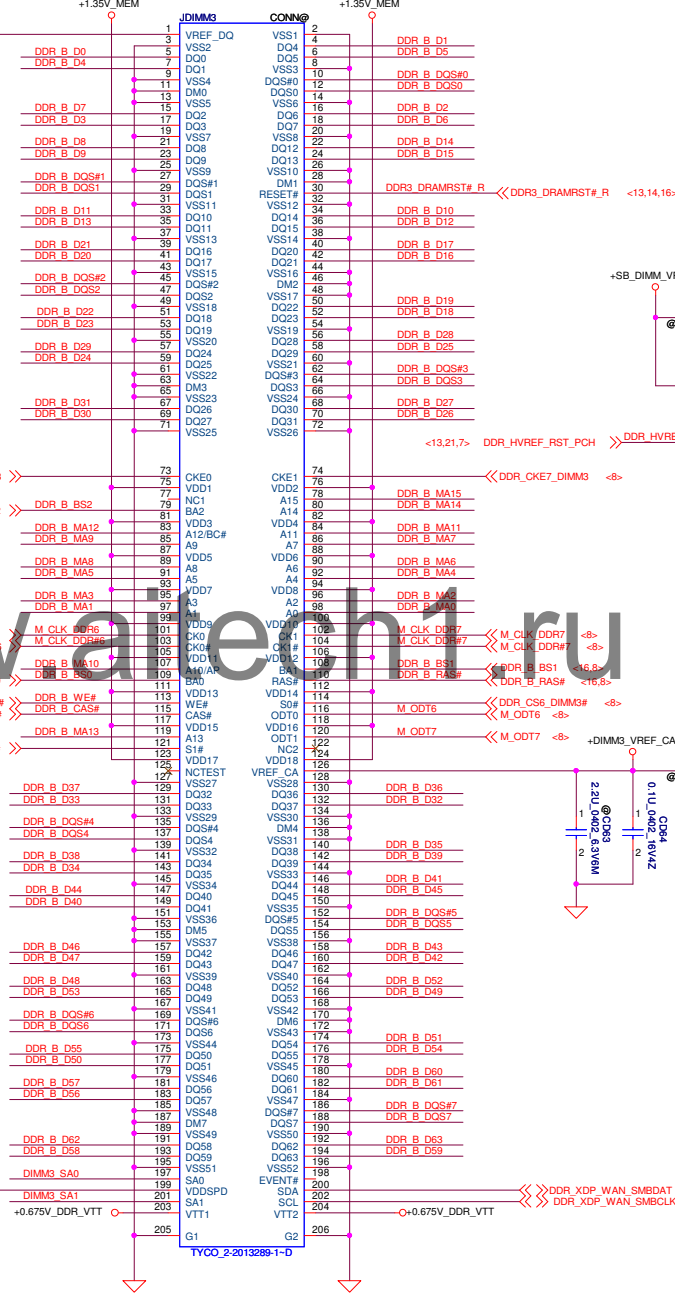
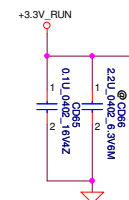
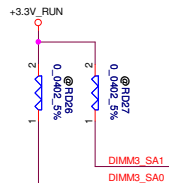


Layout Note:
Place near JDIMM3. Pin 203,204



DIMM Select

	SA0	SA1
DIMM2	0	0
DIMM4	0	1
DIMM1	1	0
DIMM3	1	1



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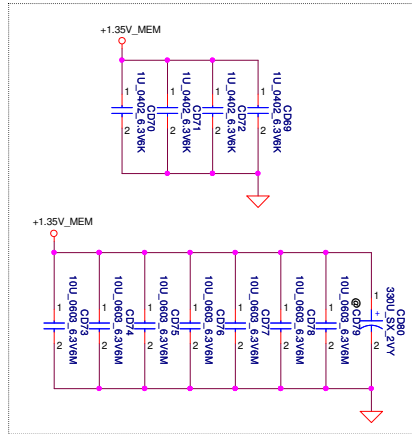
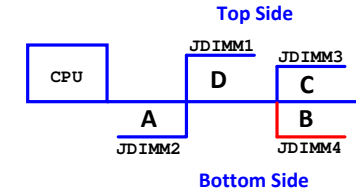
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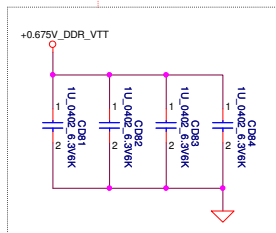
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 <15.8> DDR_B_DQ(0.7) <<>
 <15.8> DDR_B_D[0.63] <<>
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All VREF traces should
 have 10 mil trace width

JDIMM4 REV Type H=5.2

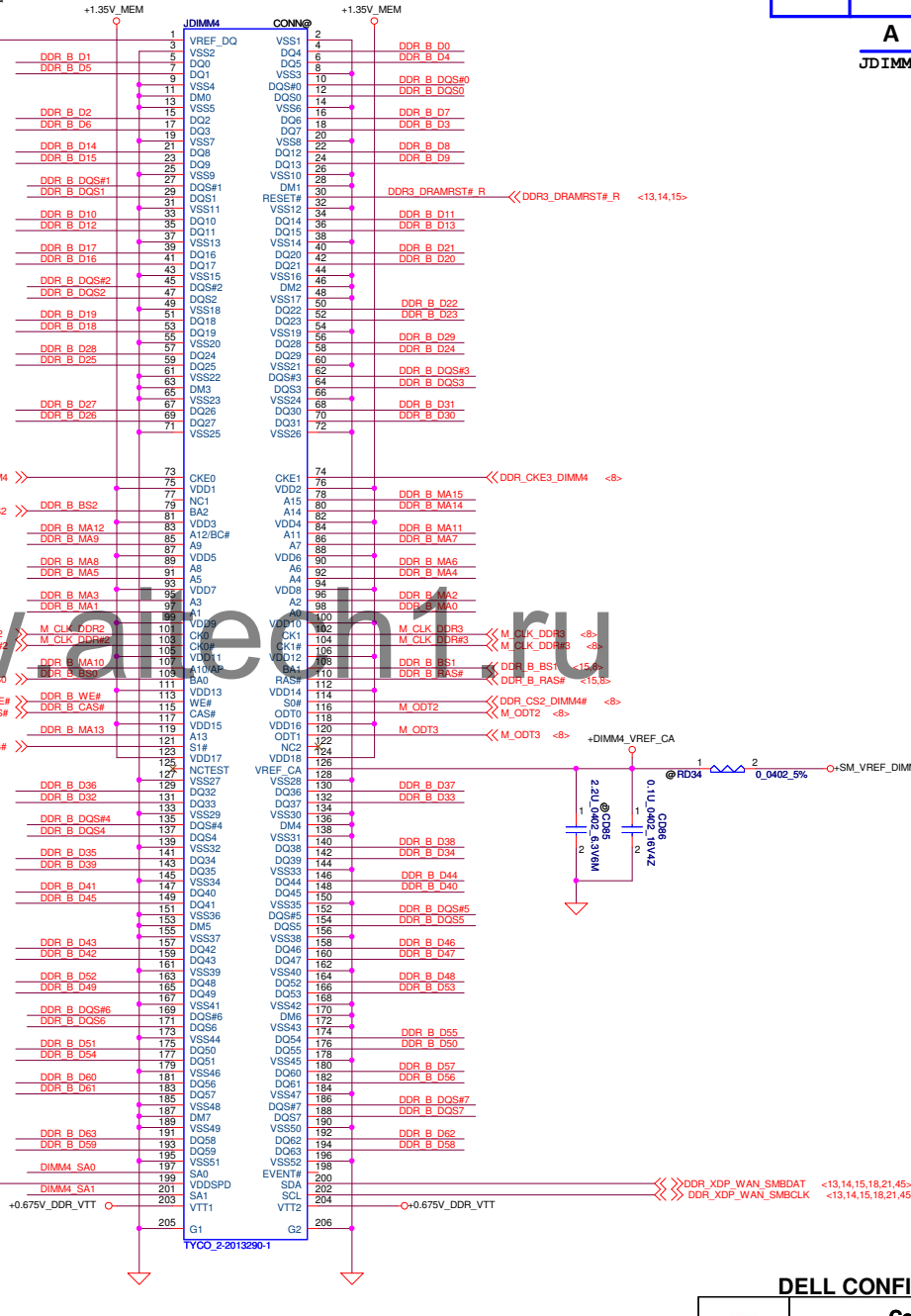
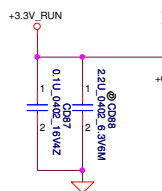
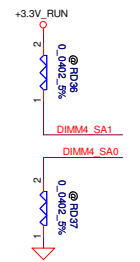


Layout Note:
 Place near JDIMM4.Pin 203,204



DIMM Select

	SA0	SA1
DIMM2	0	0
DIMM4	0	1
DIMM1	1	0
DIMM3	1	1



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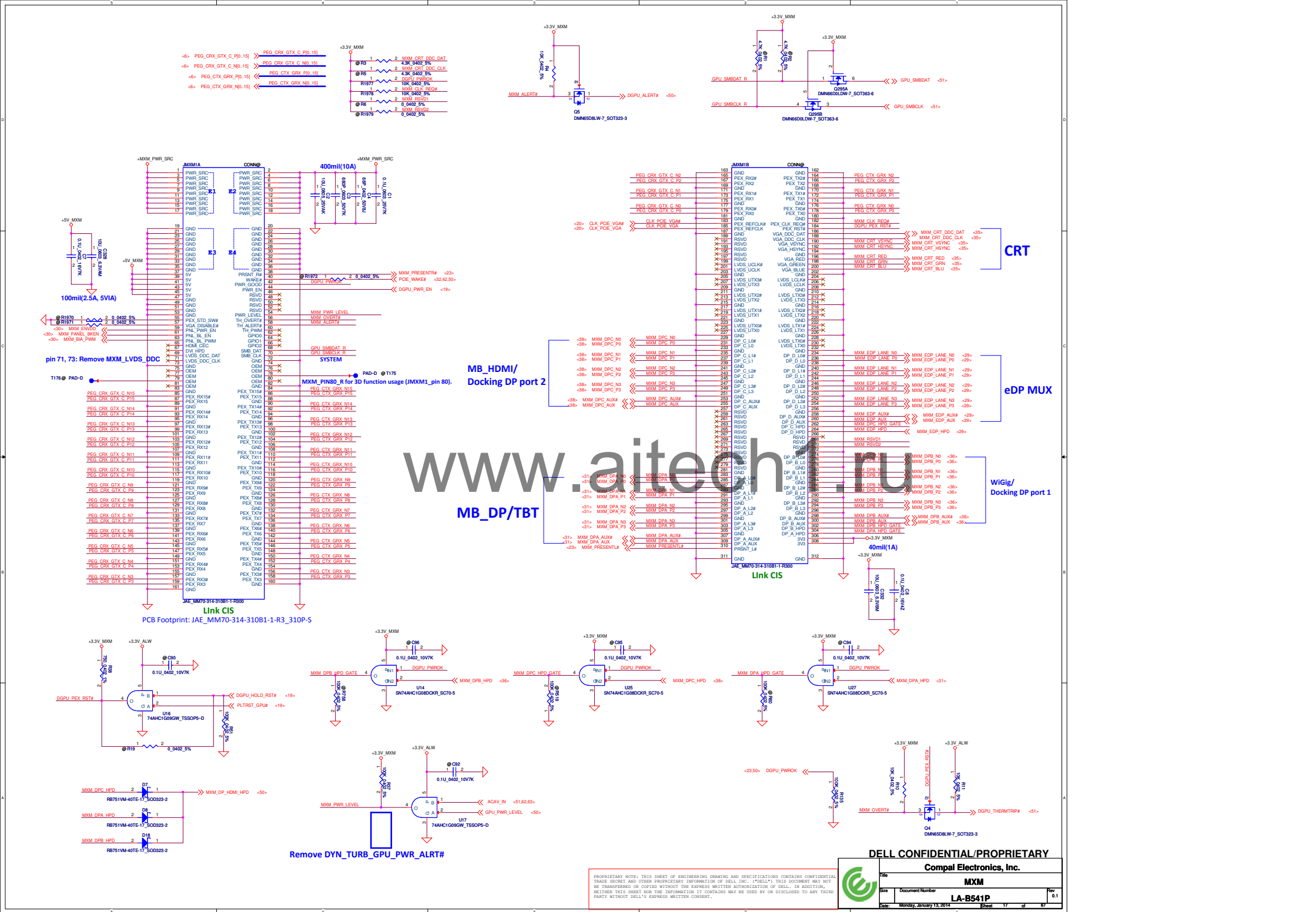
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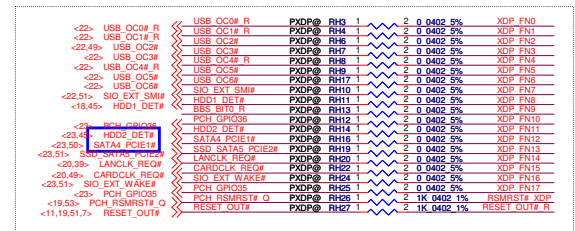
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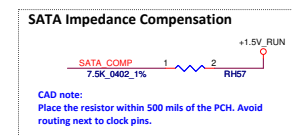
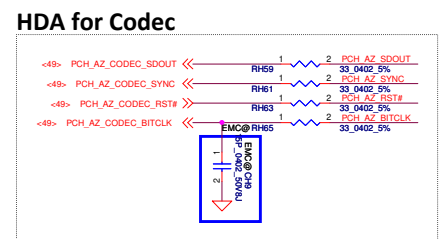
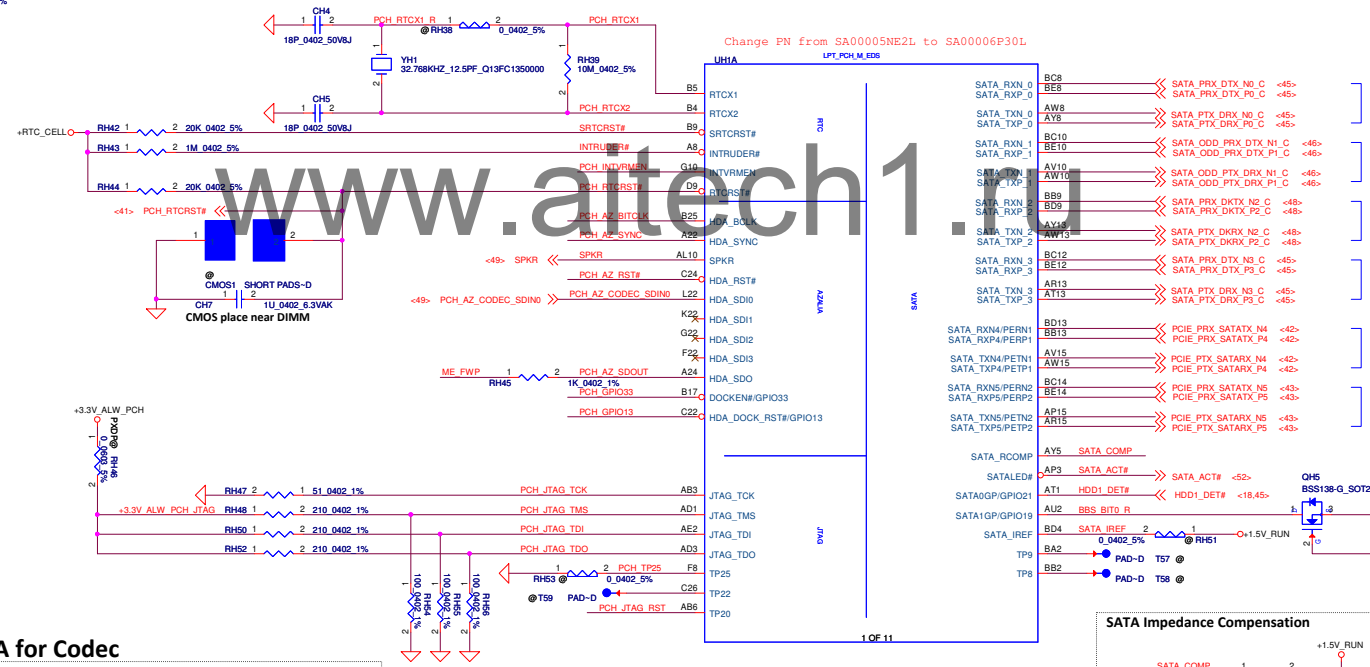
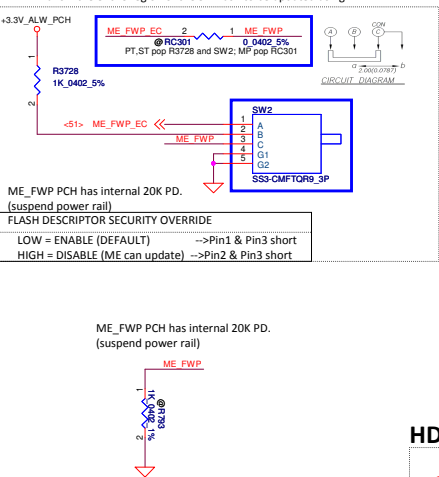
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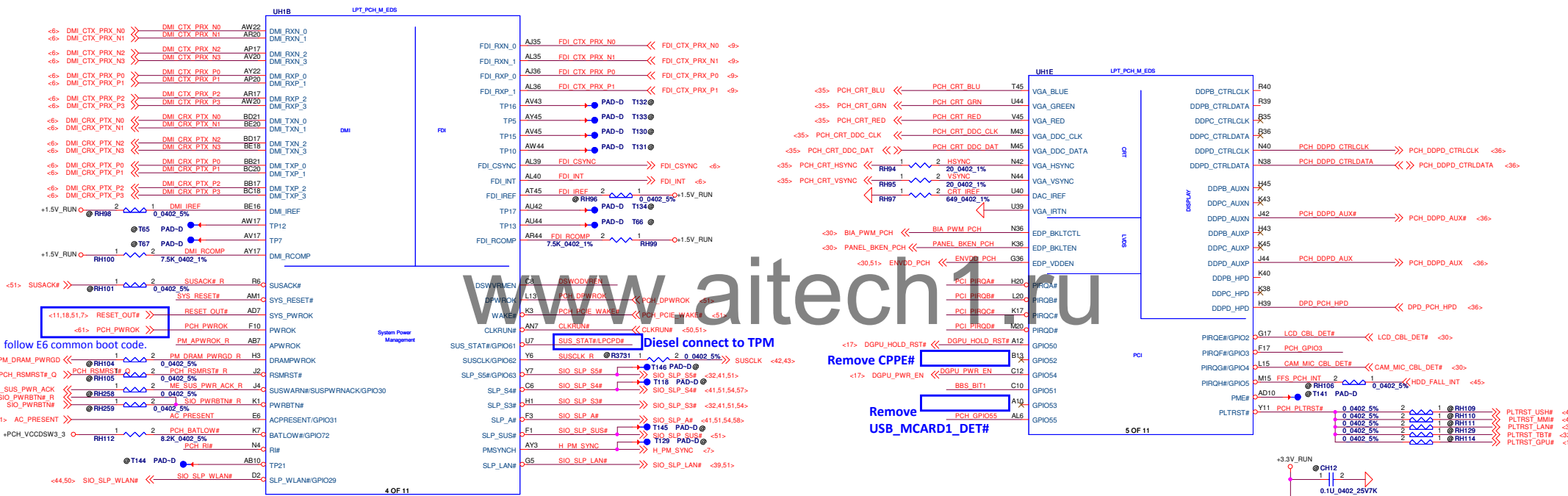


[illegible]

Service Mode Switch:
 Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.

The diagram illustrates the Service Mode Switch circuit. A 3.3V_ALW_PCH supply is connected to a resistor R3728 (1K_0402_5%) and a switch SW2. The switch SW2 is a 2-position switch with pins 1, 2, 3, 4, 5, and G2. Pin 1 is connected to ME_FWP_EC, pin 2 to ME_FWP, and pin 3 to SW3-CMIFTOR_3P. The switch is shown in the 'ON' position, connecting ME_FWP to the SW3-CMIFTOR_3P pin.





Boot BIOS Strap		
BBS_BIT1	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Remove DGPU_PWR_EN inverter circuit.

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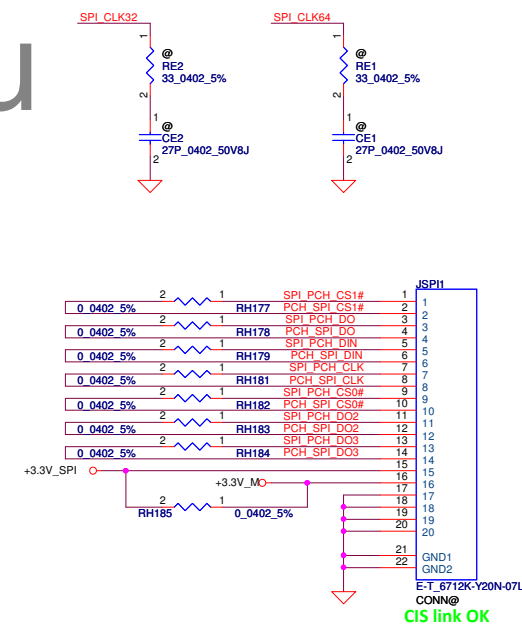
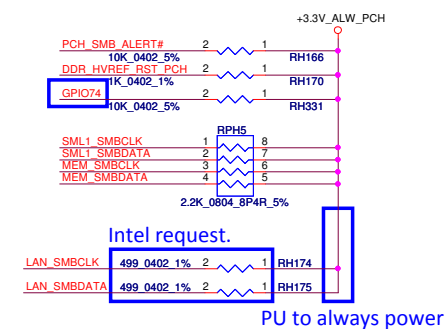
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PCH (2/9)

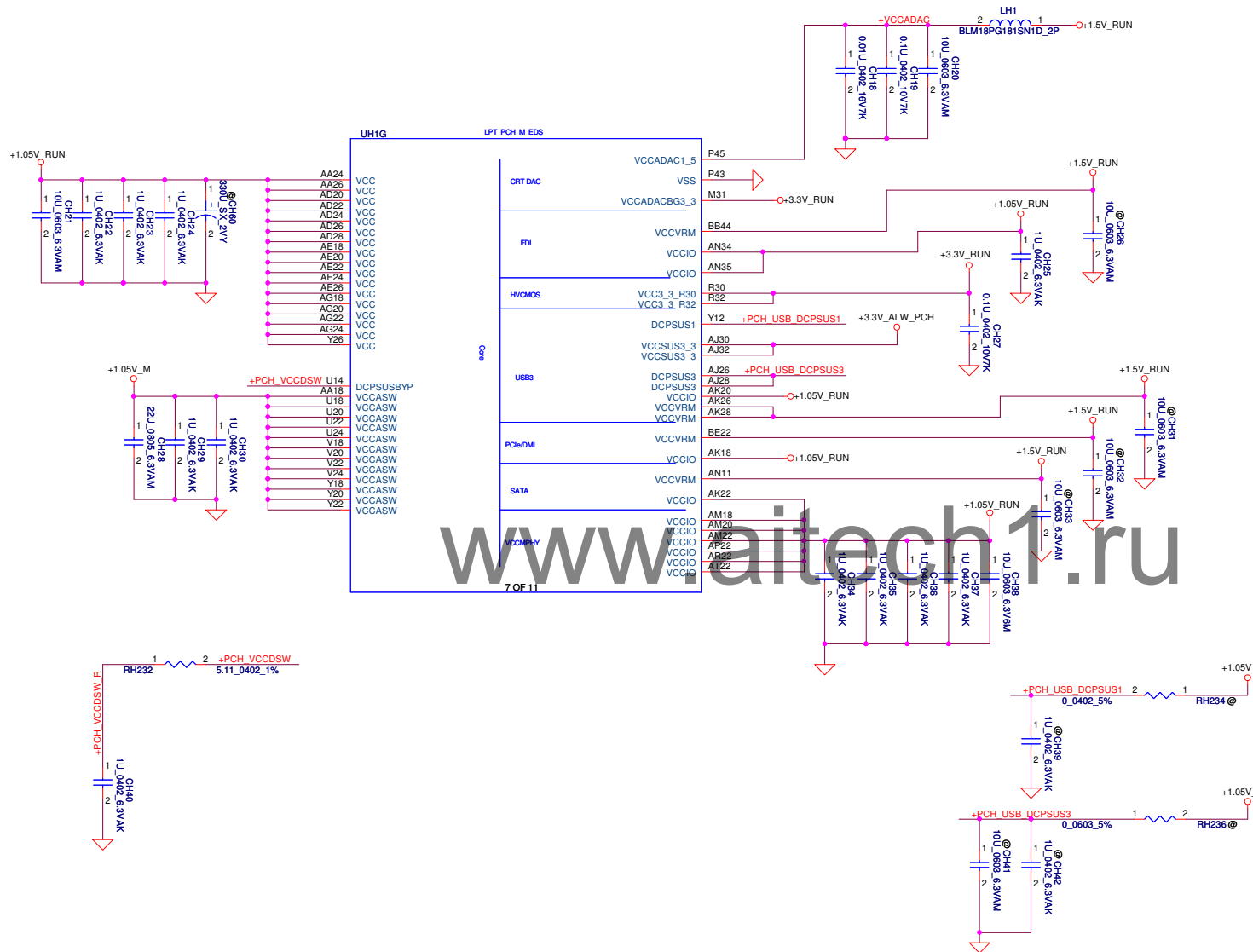
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PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCDAC1_5	1.5V	0.070 A
VCCDAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

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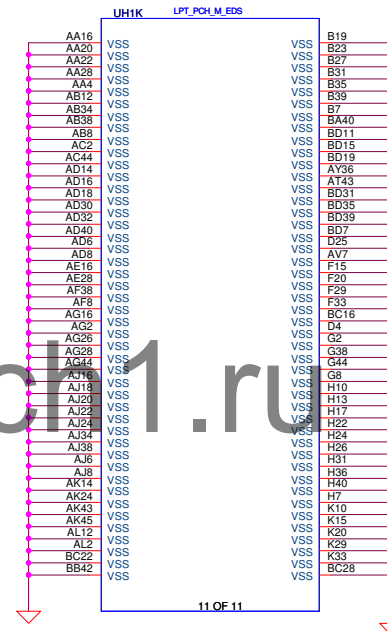
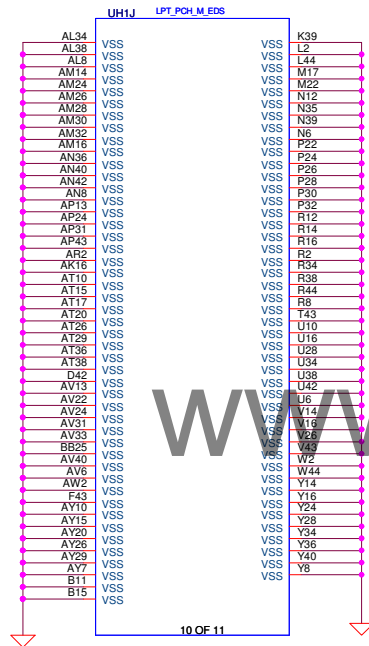


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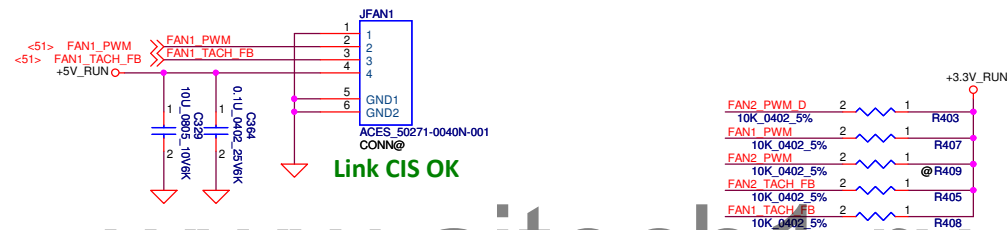
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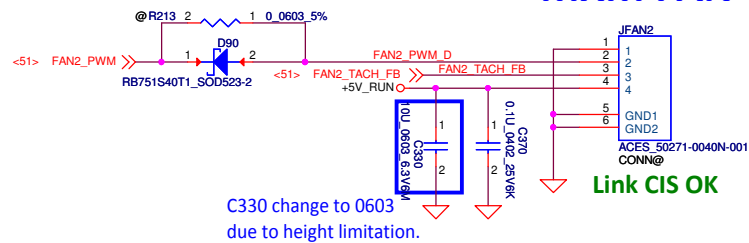
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Difference with Diesel

CPU FAN



MXM FAN



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Remove current sensor Monitor (SW solution)

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Remove current sensor Monitor (HW solution)

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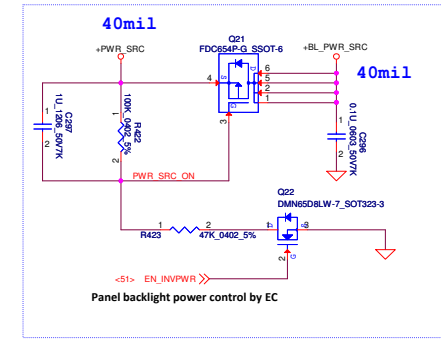
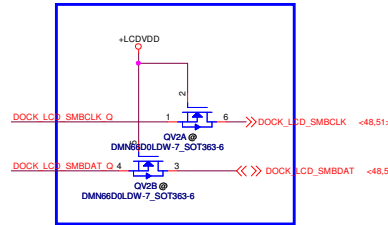
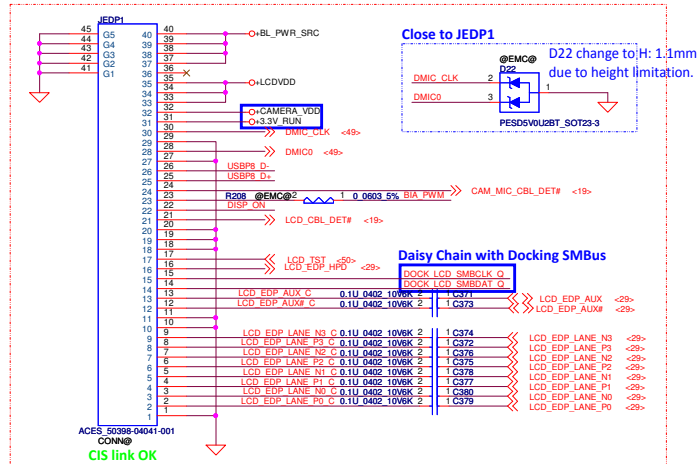


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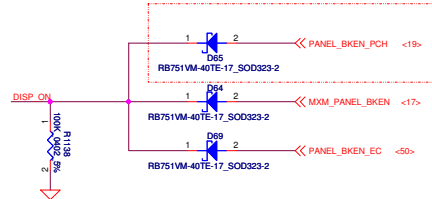
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Title		
Current Sensor		
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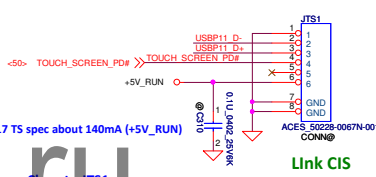
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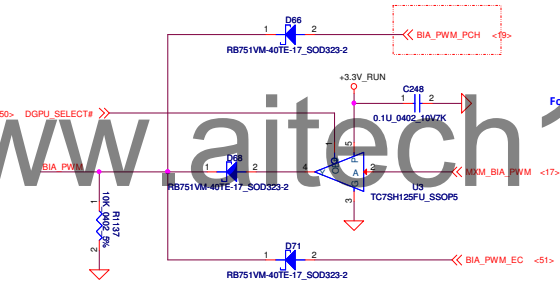
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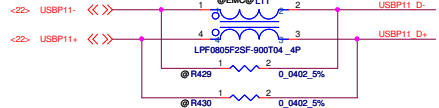
Touch Screen



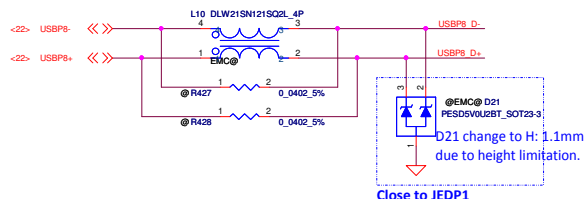
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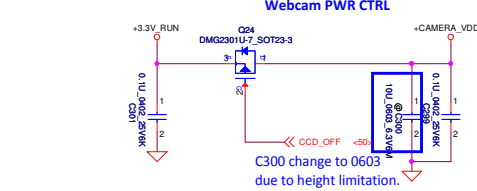
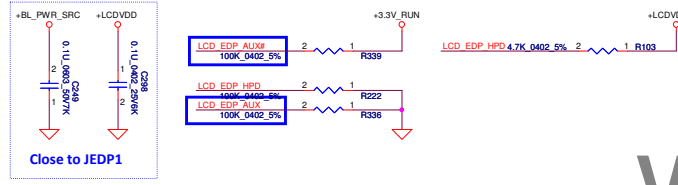
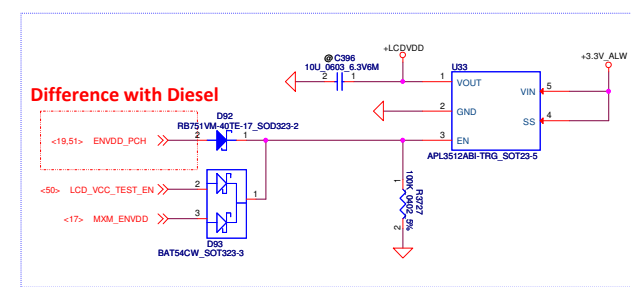
EMC request change main source to SM070002I00



EMC request change main source to SM070001N00



LCD Power



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eDP / CAM / TS

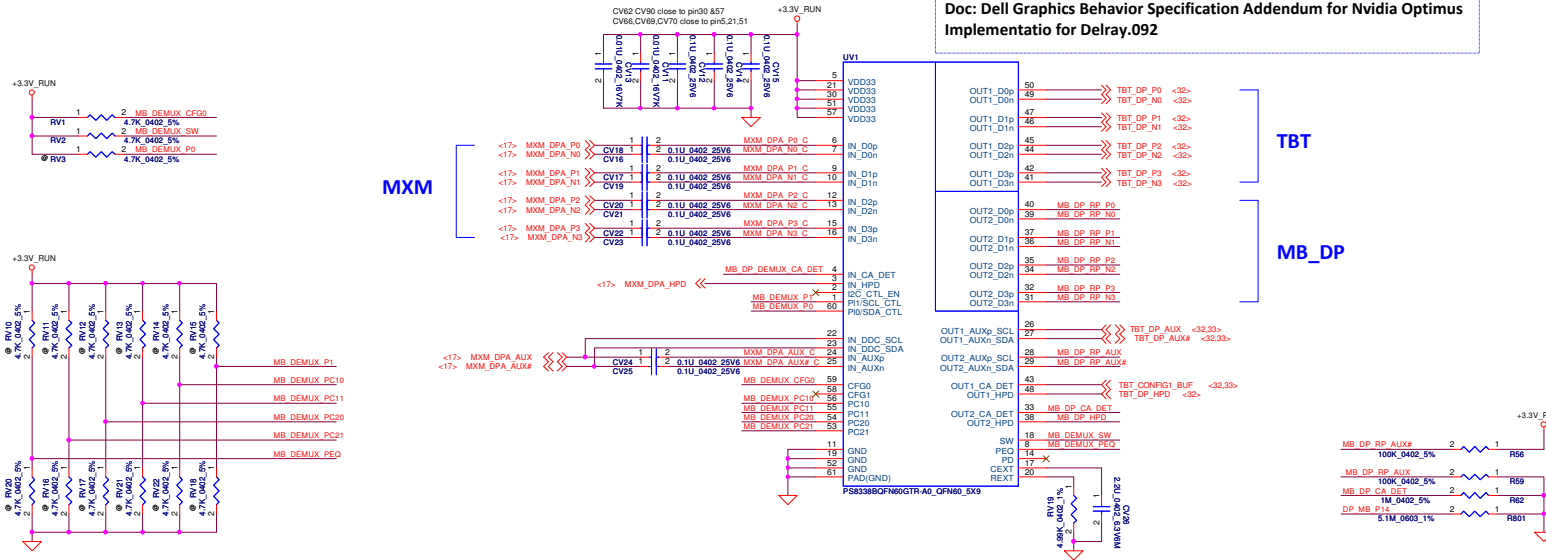
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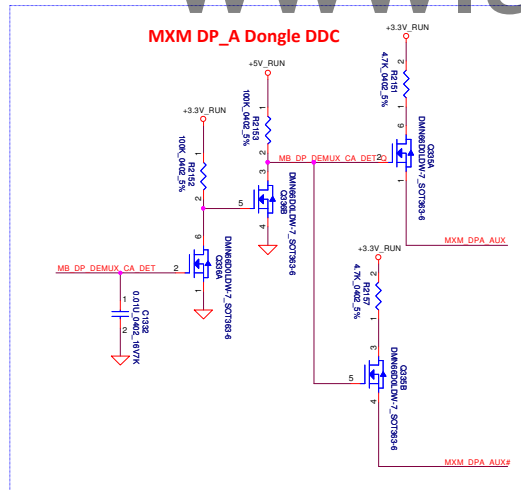
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MB_DP will have higher priority over TBT.

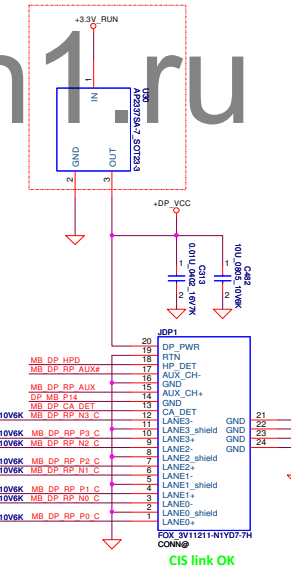
Doc: Dell Graphics Behavior Specification Addendum for Nvidia Optimus Implementatio for Delay.092



MXM DP_A Dongle DDC



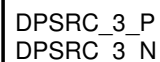
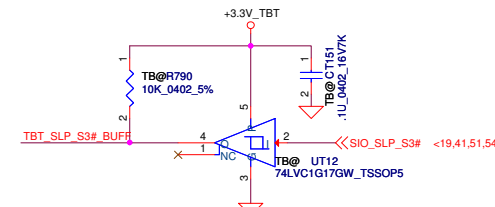
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DP SW (PS8338) & DP Conn	
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Remove BATT low CKT

Design guide:
1*100u
1*22u
1*0.1u

EN	HV_EN	OUT
0	0	OPEN
0	1	OPEN
1	0	V3P3
1	1	VHV

Current design (12V) = 1.06A
Current design (3V) = 1.18A

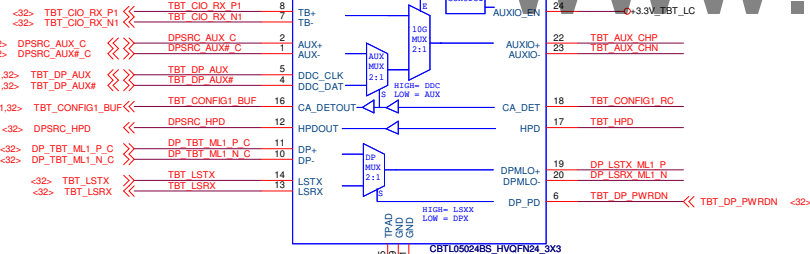
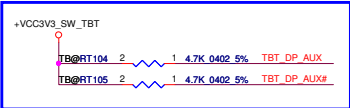


Table 3-1. Cable Type Indications

HPD	CONFIG1	CONFIG2	LSRX	Cable Type	Comments
0	X	0	X	None	Cable is disconnected
1	0	0	X	DisplayPort	
1	1	X	X	DVI/HDMI	Host/Source software determines DVI or HDMI
0	0	1	0	Thunderbolt	Thunderbolt Technology cable attached but no Thunderbolt Host/Device attached
0	0	1	1	Thunderbolt	Thunderbolt Technology operation

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Title BWD-TBT-LP(2/3) HOST.mDP

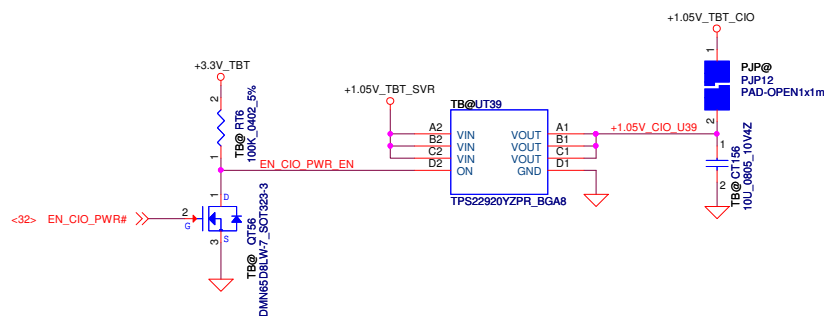
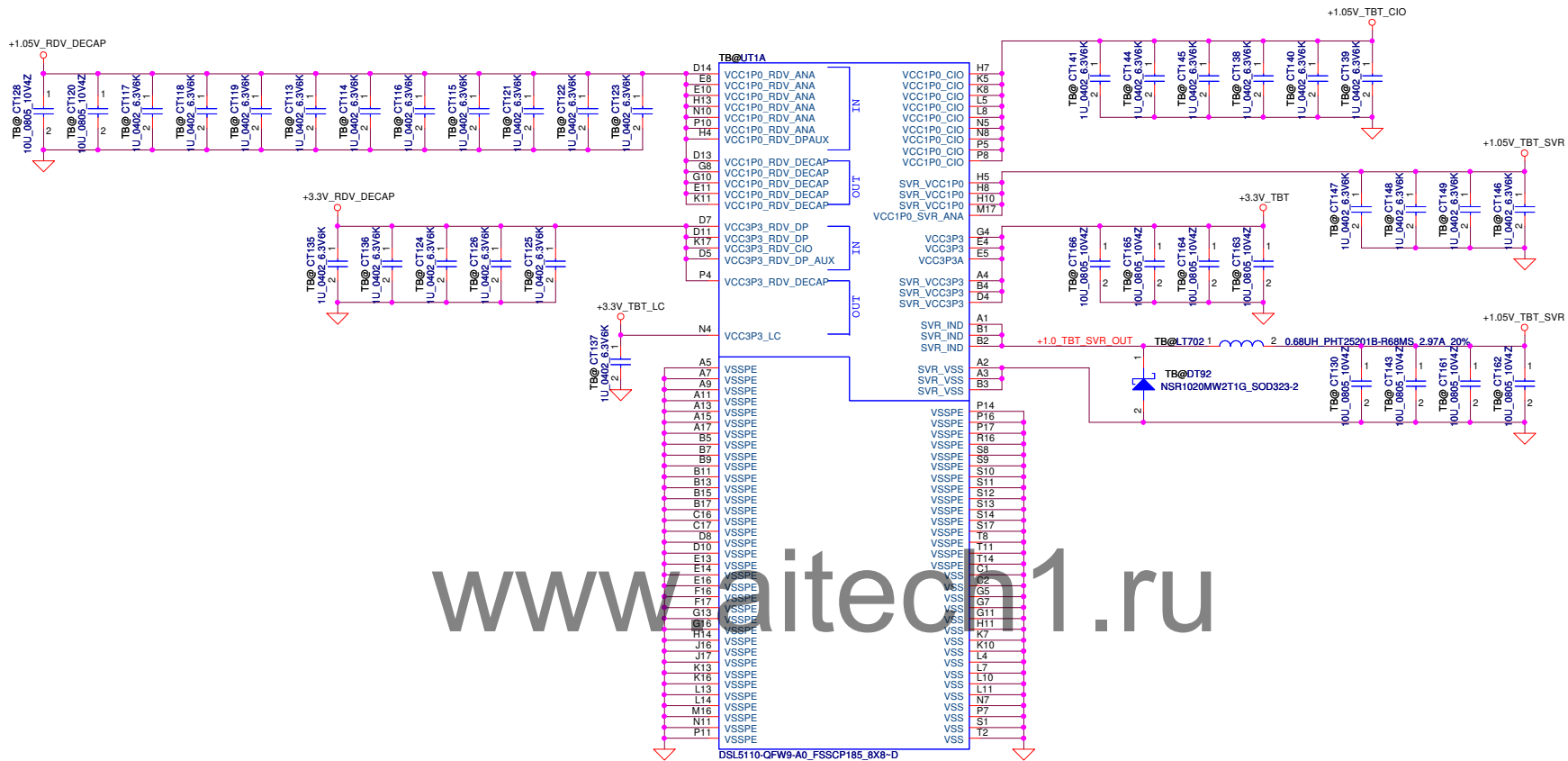
Size Document Number

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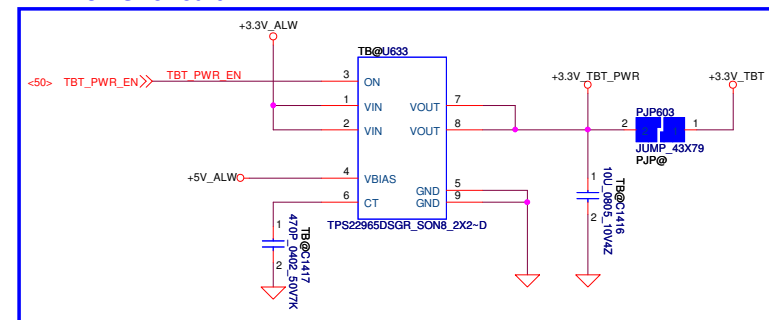
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2012/10/18 INTER: this 12.1 ohm is still required for JAB or Lintex TBT connector

CIS link OK



TBT Power circuit



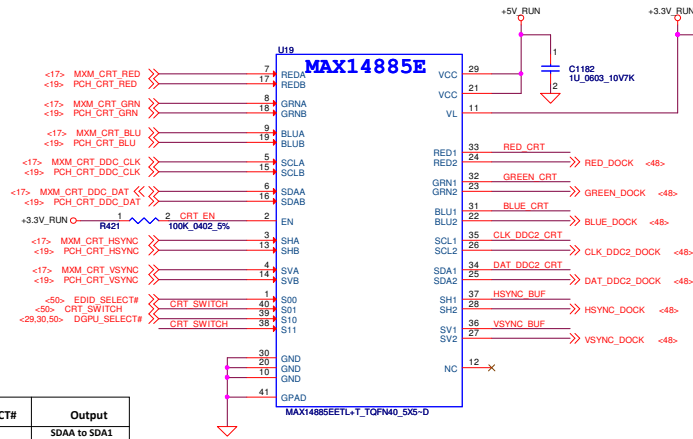
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BWD-TBT-LP(3/3) VCC/VSS			
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Channel A (MXM)

Channel B (PCH)

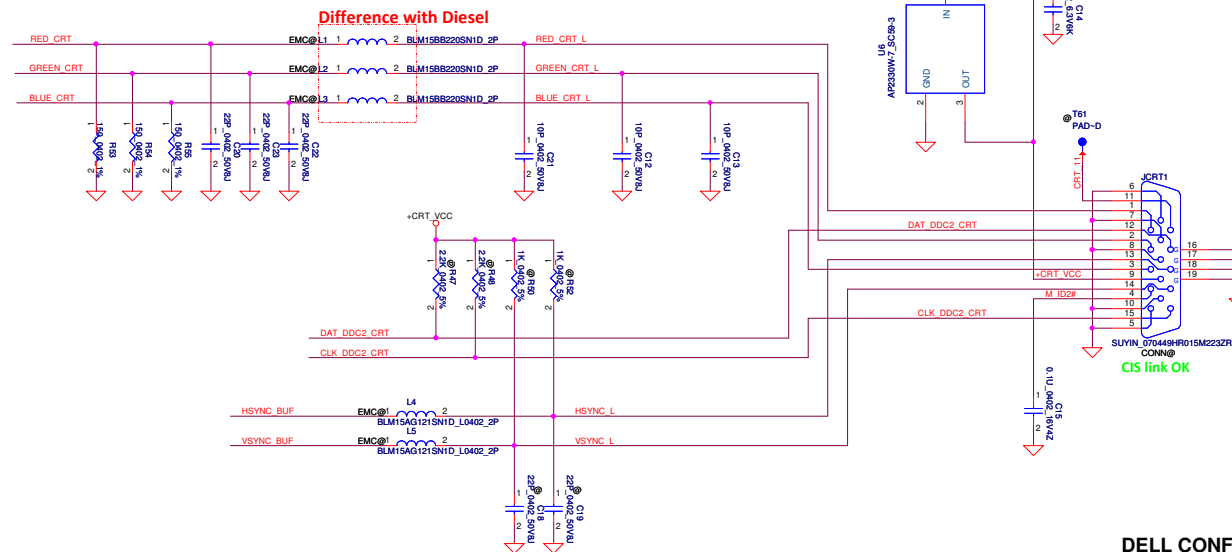


Port 1 (MB_CRT)

Port 2 (Dock_CRT)

	CRT_SWITCH	DGPU_SELECT#	EDID_SELECT#	Output
DSC mode output to MB VGA	0	0	0	SDAA to SDA1 SCLA to SCL1 REDA to RED1 GRNA to GRN1 BLUA to BLU1 SHA to SH1 SVA to SV1
DSC mode output to docking VGA	1	0	0	SDAA to SDA2 SCLA to SCL2 REDA to RED2 GRNA to GRN2 BLUA to BLU2 SHA to SH2 SVA to SV2
UMA mode output to MB VGA	0	1	1	SDAB to SDA1 SCLB to SCL1 REDB to RED1 GRNB to GRN1 BLUB to BLU1 SHB to SH1 SVB to SV1
UMA mode output to docking VGA	1	1	1	SDAB to SDA2 SCLB to SCL2 REDB to RED2 GRNB to GRN2 BLUB to BLU2 SHB to SH2 SVB to SV2

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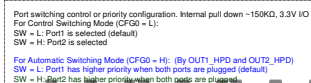
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VGA CONN

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	H	L
CFG0	V	
SW		V

* Automatic Switching Mode (CFG0 = H): (By OUT1, HPD and OUT2, HPD)
 * L-Port1 has higher priority when both ports are plugged (default)
 * H-Port2 has higher priority when both ports are plugged

CFG0	V		
SW			V

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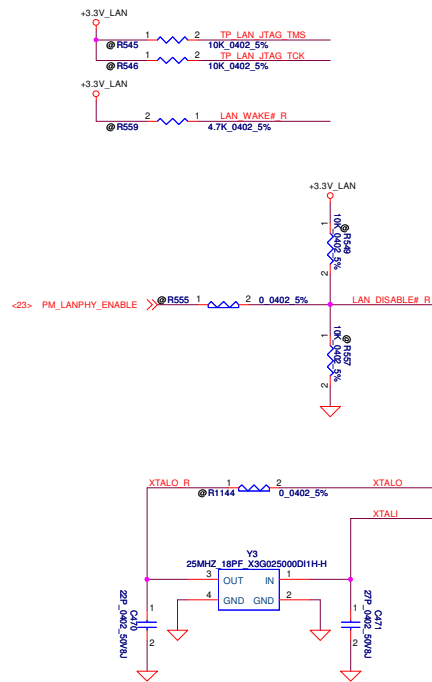
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DP DeMUX (PS8338)

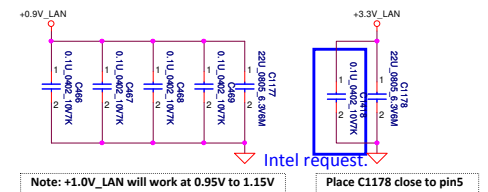
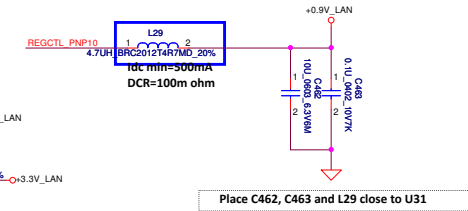
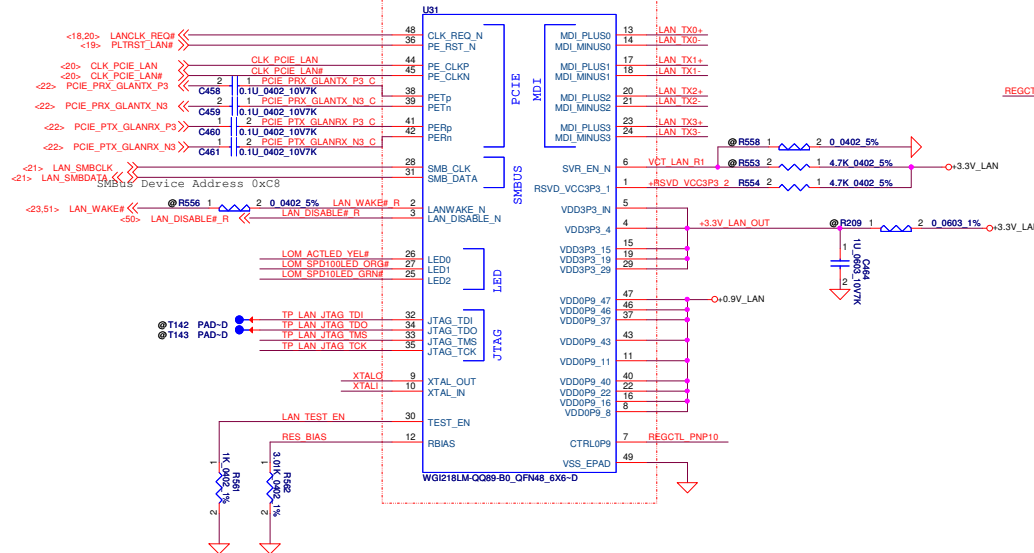
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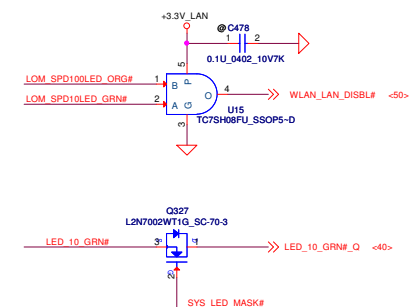
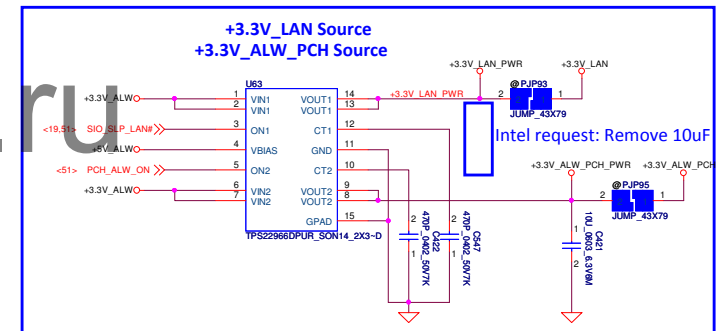
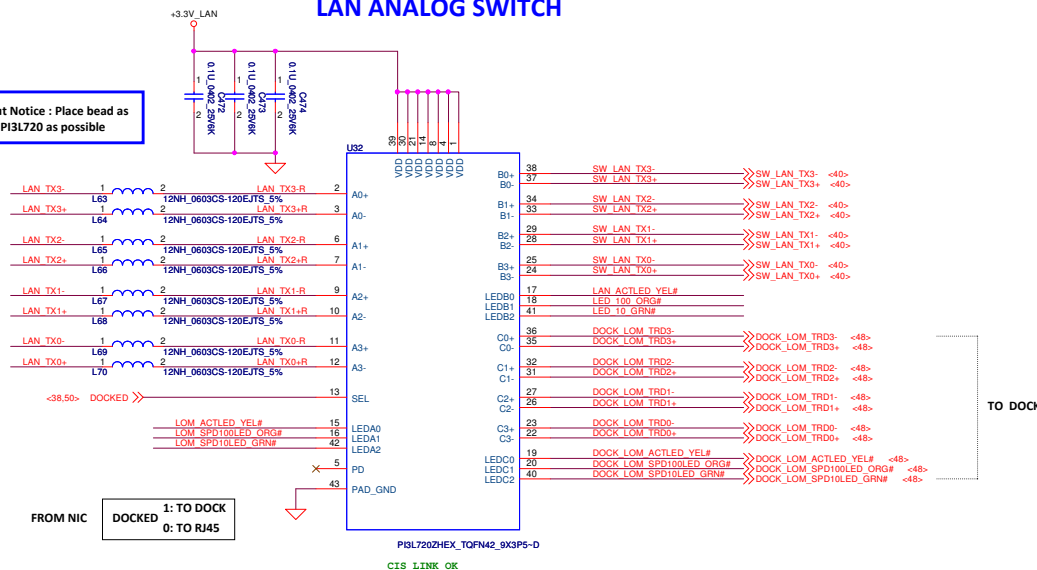
Difference with Diesel



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LAN ANALOG SWITCH

Layout Notice : Place bead as close P13L720 as possible



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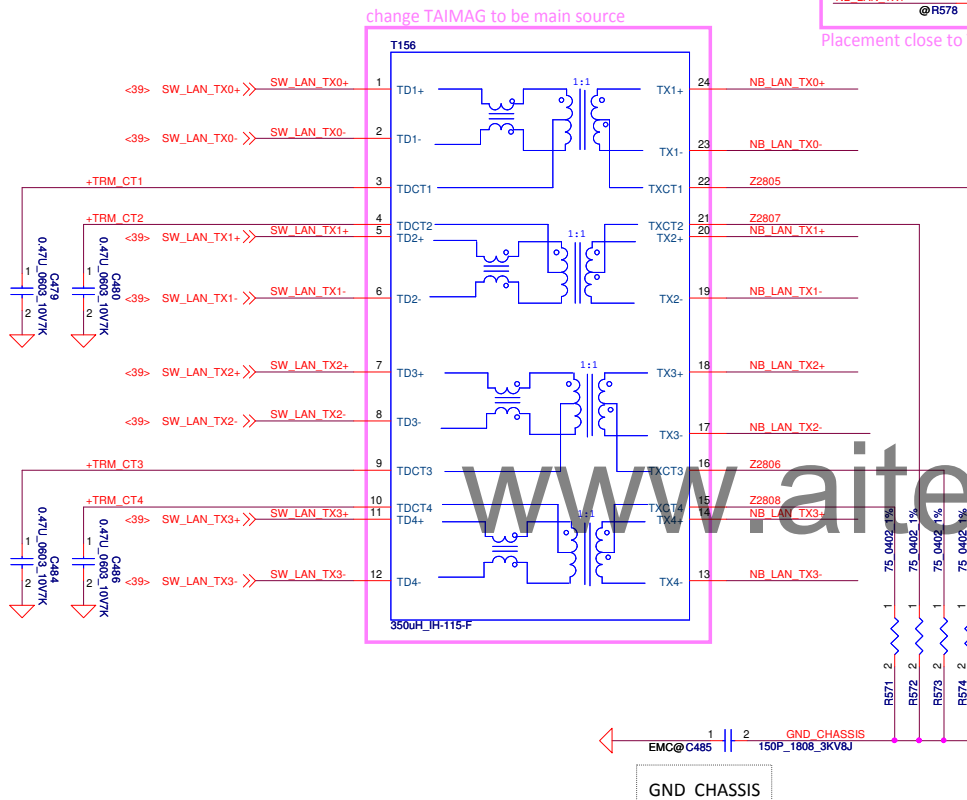
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LAN/LAN SW

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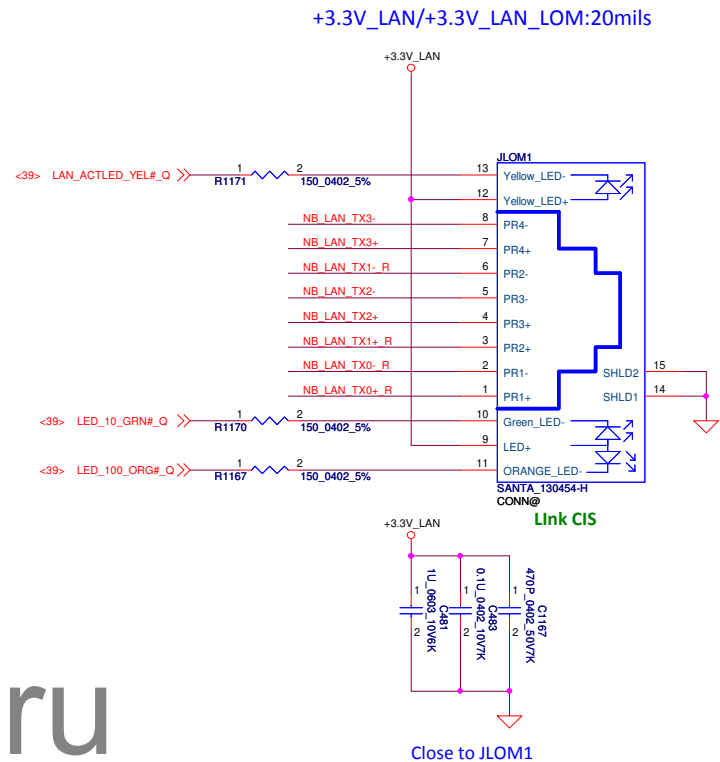
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For IEEE EA request

NB_LAN_TX0+	1	2	0.0402_5%	NB_LAN_TX0+ R
NB_LAN_TX0-	1	2	0.0402_5%	NB_LAN_TX0- R
NB_LAN_TX1+	1	2	0.0402_5%	NB_LAN_TX1+ R
NB_LAN_TX1-	1	2	0.0402_5%	NB_LAN_TX1- R
NB_LAN_TX2+	1	2	0.0402_5%	NB_LAN_TX2+ R
NB_LAN_TX2-	1	2	0.0402_5%	NB_LAN_TX2- R
NB_LAN_TX3+	1	2	0.0402_5%	NB_LAN_TX3+ R
NB_LAN_TX3-	1	2	0.0402_5%	NB_LAN_TX3- R

Placement close to T156



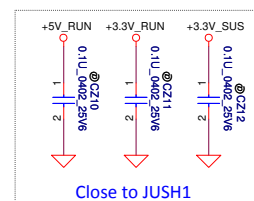
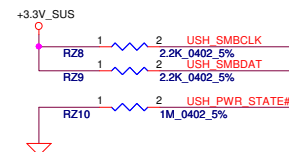
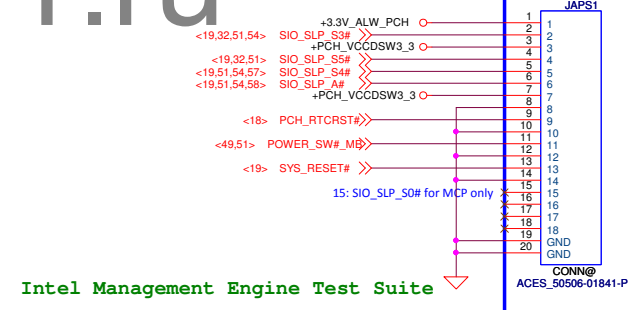
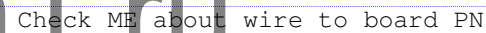
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RJ45

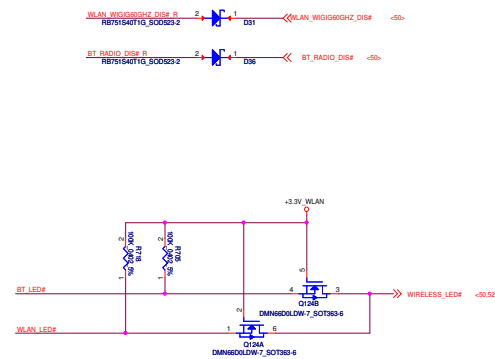
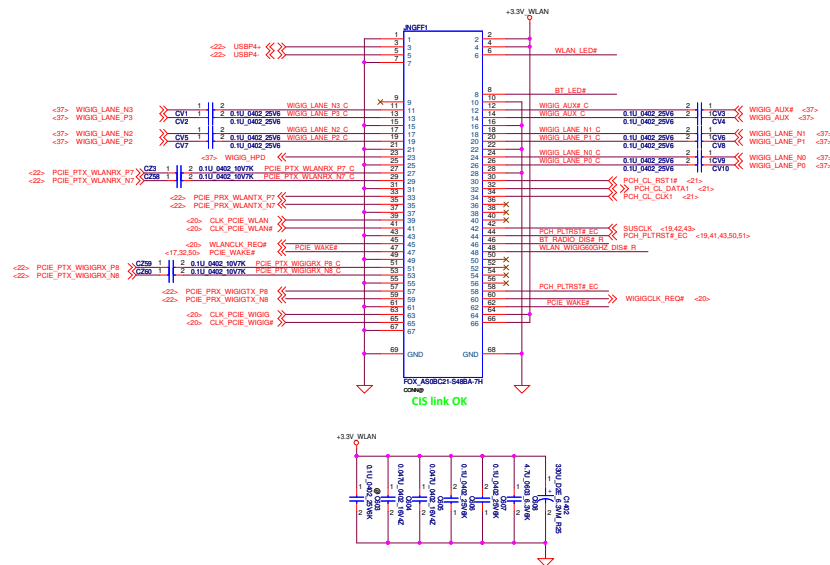
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Document Number		0.1	
LA-B541P			
Date:	Monday, January 13, 2014	Sheet	40 of 67

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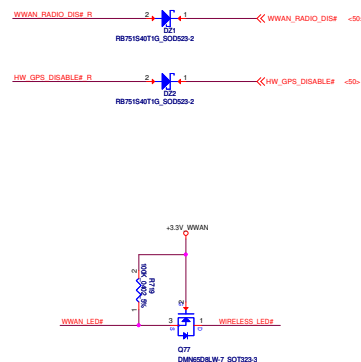
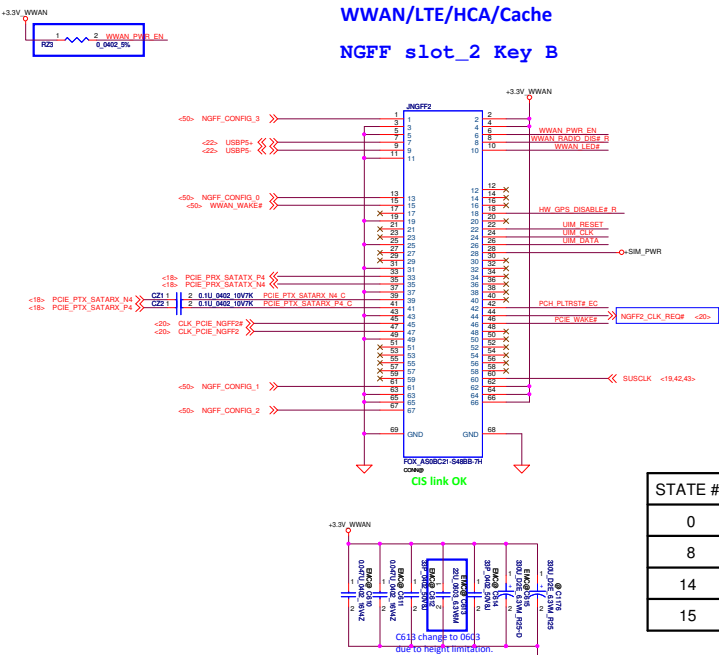
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	TPM/USH		
	Size	Document Number	Rev
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Date: Monday, January 13, 2014		Sheet 41 of 67	

WLAN/BT/WiGig NGFF slot_1 Key A

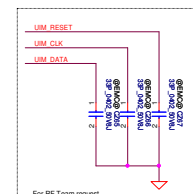
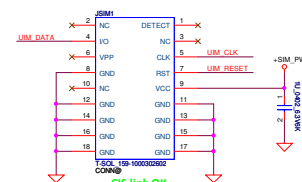


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WWAN/LTE/HCA/Cache NGFF slot_2 Key B



SIM Card Push-Push



STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	0	0	0	0	SSD-SATA
8	1	0	0	0	WWAN
14	1	0	1	1	HCA-PCIE
15	1	1	1	1	NA

C615 footprint change to C_APXK2R5ARA331MF451

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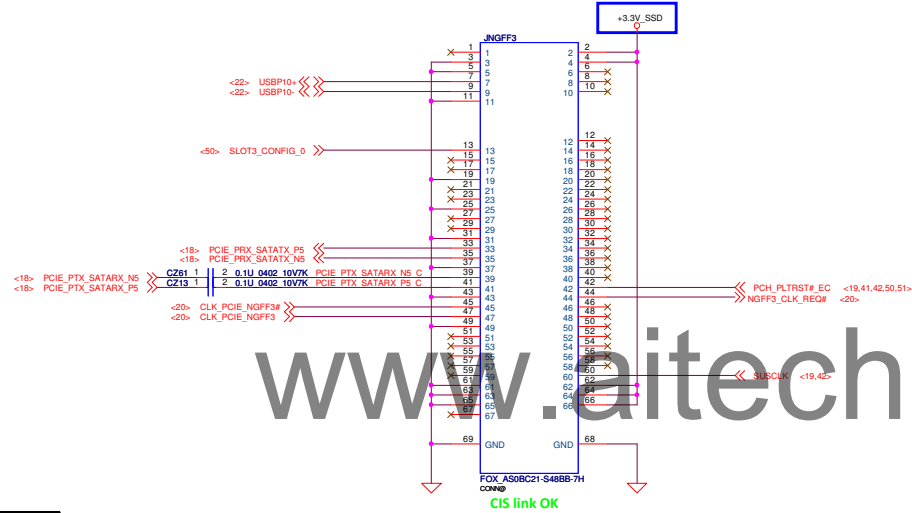
M.2 Card-1/2

LA-B541P

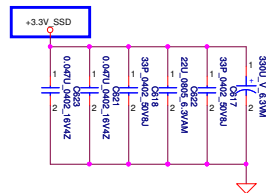


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SSD/HCA/Cache NGFF slot_3 Key B



STATE #	CONFIG_0	Module Type
0	0	SSD-SATA
14	1	HCA-PCIE



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M.2 Card-2/2

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Power Control for M.2 slot 1. & +3.3V_RUN Source

The diagram illustrates the connection of the TPS22965DSGR_SON8_2X2-D (U43) in a 2x2 configuration. The chip's pins are connected as follows:

- Pin 1 (ON):** Connected to the 3.3V_WWAN_EN signal.
- Pin 2 (VIN):** Connected to the 3.3V_ALW supply.
- Pin 3 (VIN):** Connected to the 3.3V_WWAN_EN signal.
- Pin 4 (VBIAS):** Connected to the +5V_ALW supply.
- Pin 5 (GND):** Connected to ground.
- Pin 6 (CT):** Connected to ground via a 470pF capacitor (C541).
- Pin 7 (VOUT):** Connected to the 3.3V_WWAN_EN signal.
- Pin 8 (VOUT):** Connected to the 3.3V_WWAN_EN signal.
- Pin 9 (GND):** Connected to ground.

Additional components and connections include:

- A 100k pull-down resistor (R720) connected to the 3.3V_WWAN_EN signal.
- A 10uF capacitor (C726) connected to the 3.3V_WWAN supply.
- A 3.3V_WWAN supply connected to the 3.3V_WWAN_EN signal.

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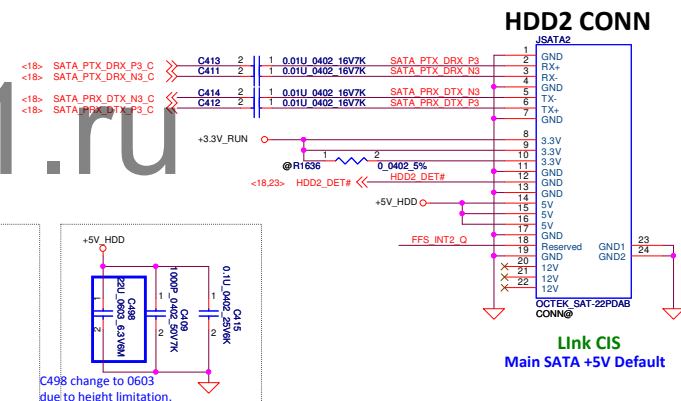
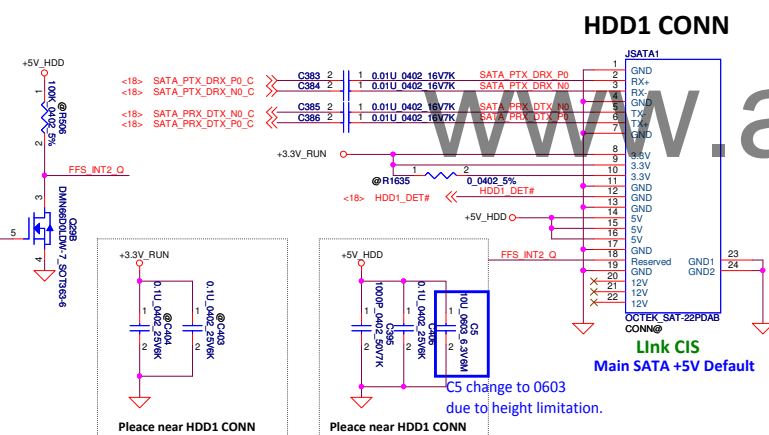
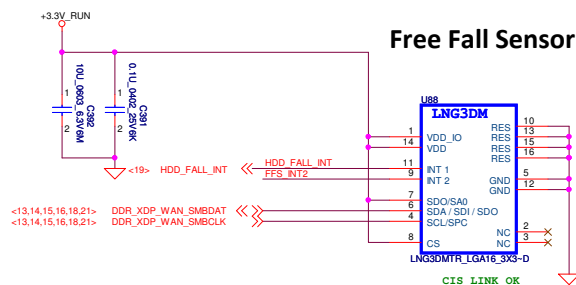
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Title	M.2 Card PWR
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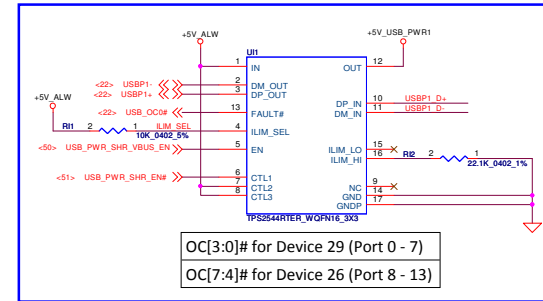
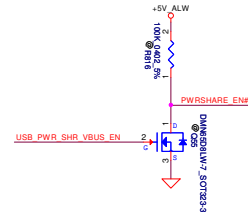
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	LA-B541P	0.1

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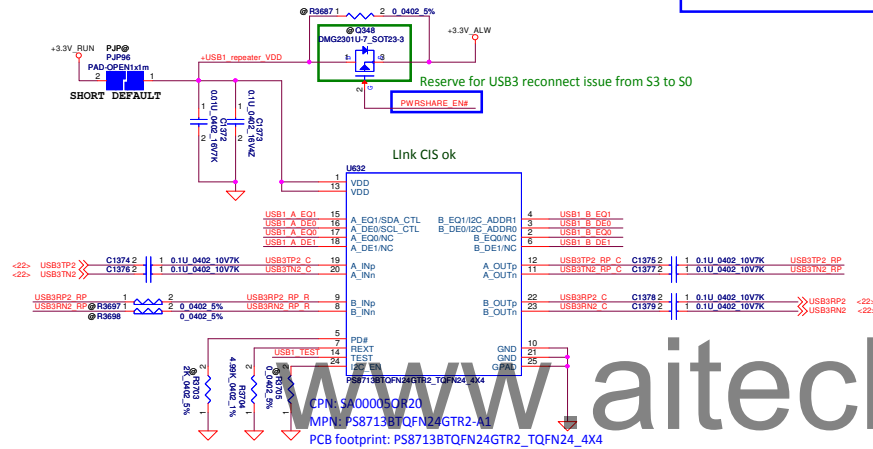
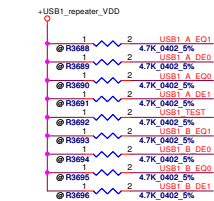
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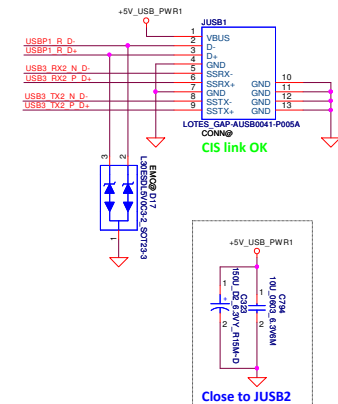
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Remove SLG55594



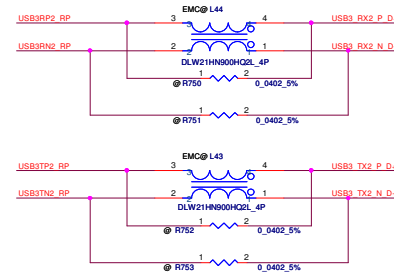
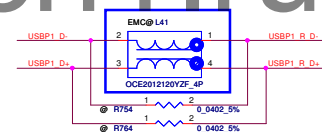
Difference with Diesel



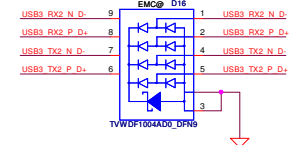
Parade_PS8713B

A_EQ0	A_EQ1	B_EQ0	B_EQ1	Recommended EQ
0	0	0	0	loss up to 9.5dB
0	1	0	1	loss up to 4.5dB
1	0	1	0	loss up to 13dB
1	1	1	1	loss up to 7.5dB

Both A_EQ0&B_EQ0 have internal pull-down 150K



For ESD request



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USB3.0

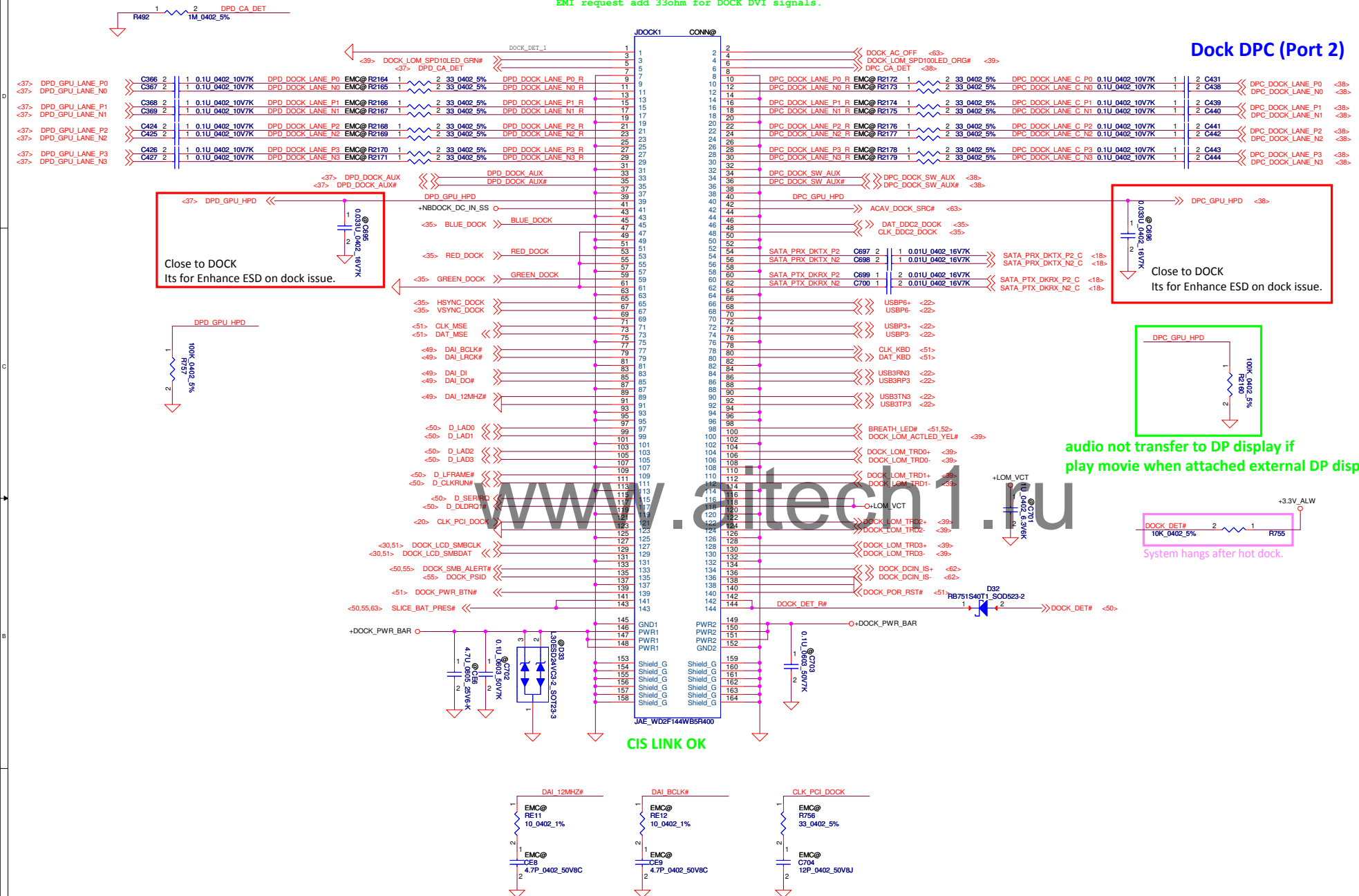
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EMI request add 33ohm for DOCK DVI signals.

Dock DPC (Port 2)



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Docking

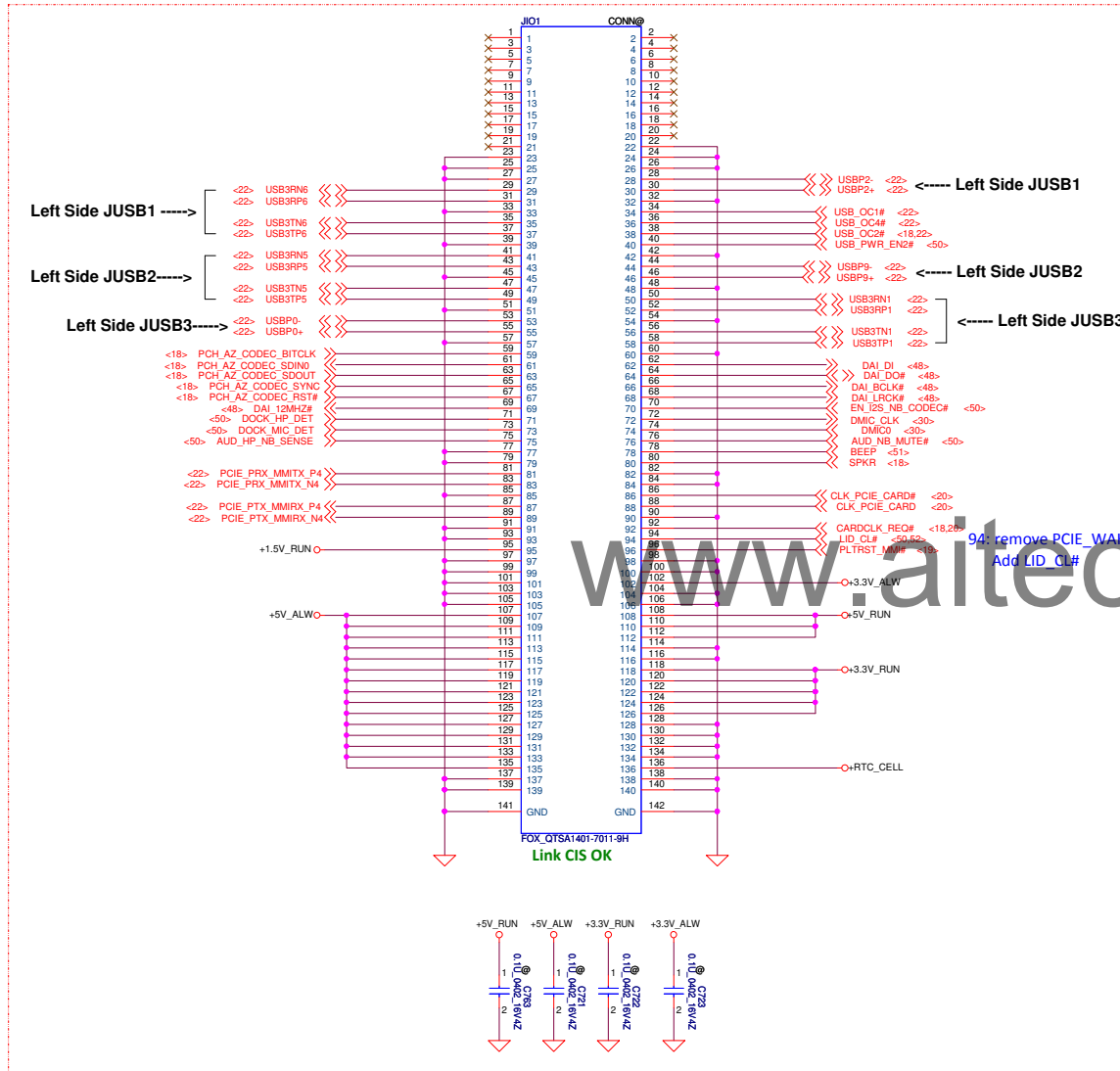
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Date: Monday, January 13, 2014

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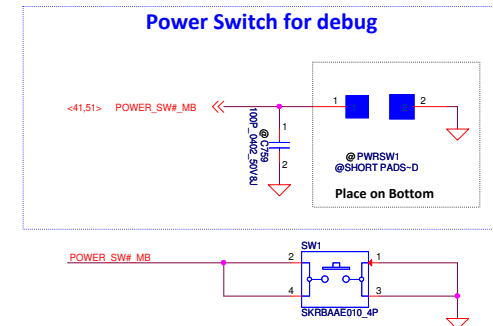
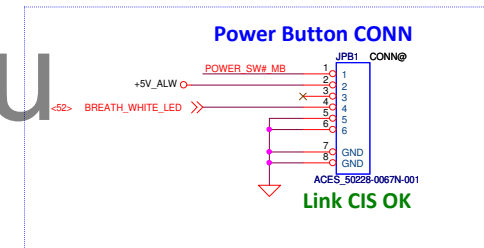
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Difference with Diesel



Difference with Diesel

WireLess ON/OFF CONN



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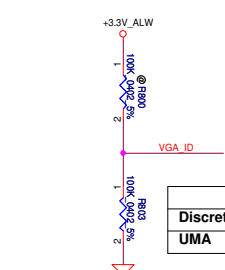
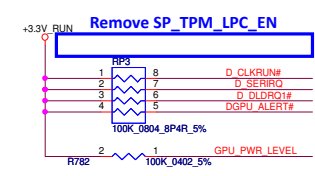
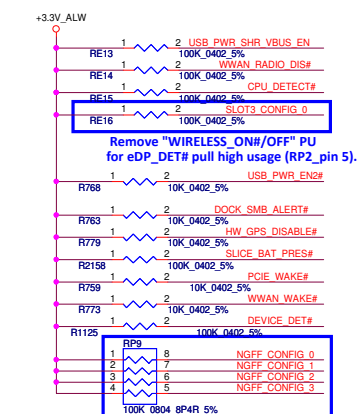
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File
IO / PWR Button

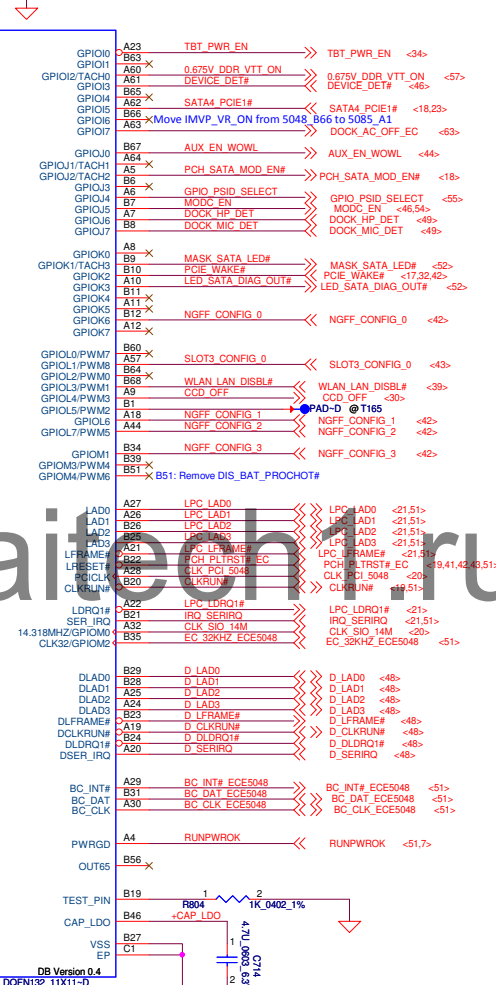
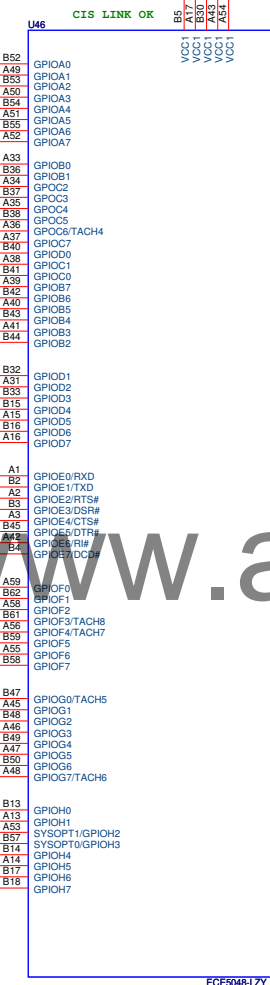
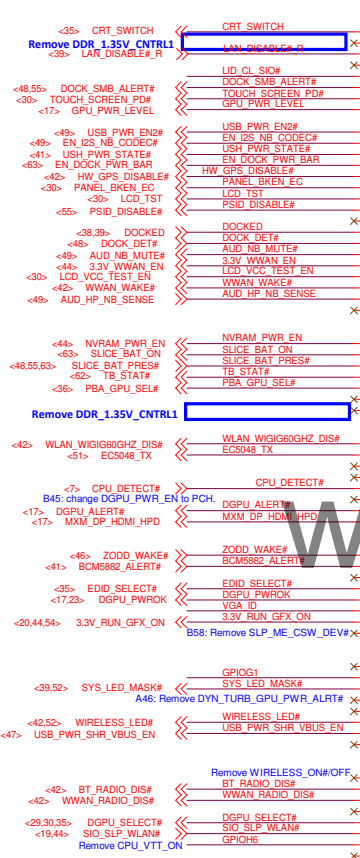
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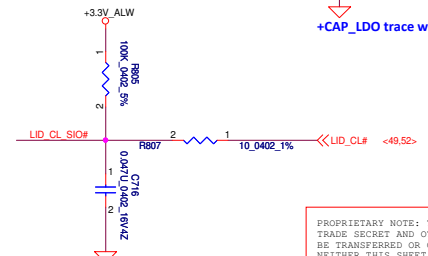
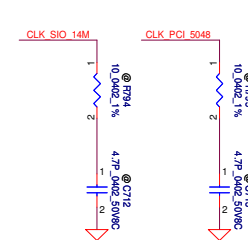
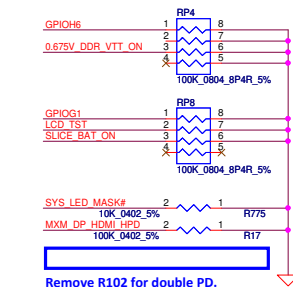
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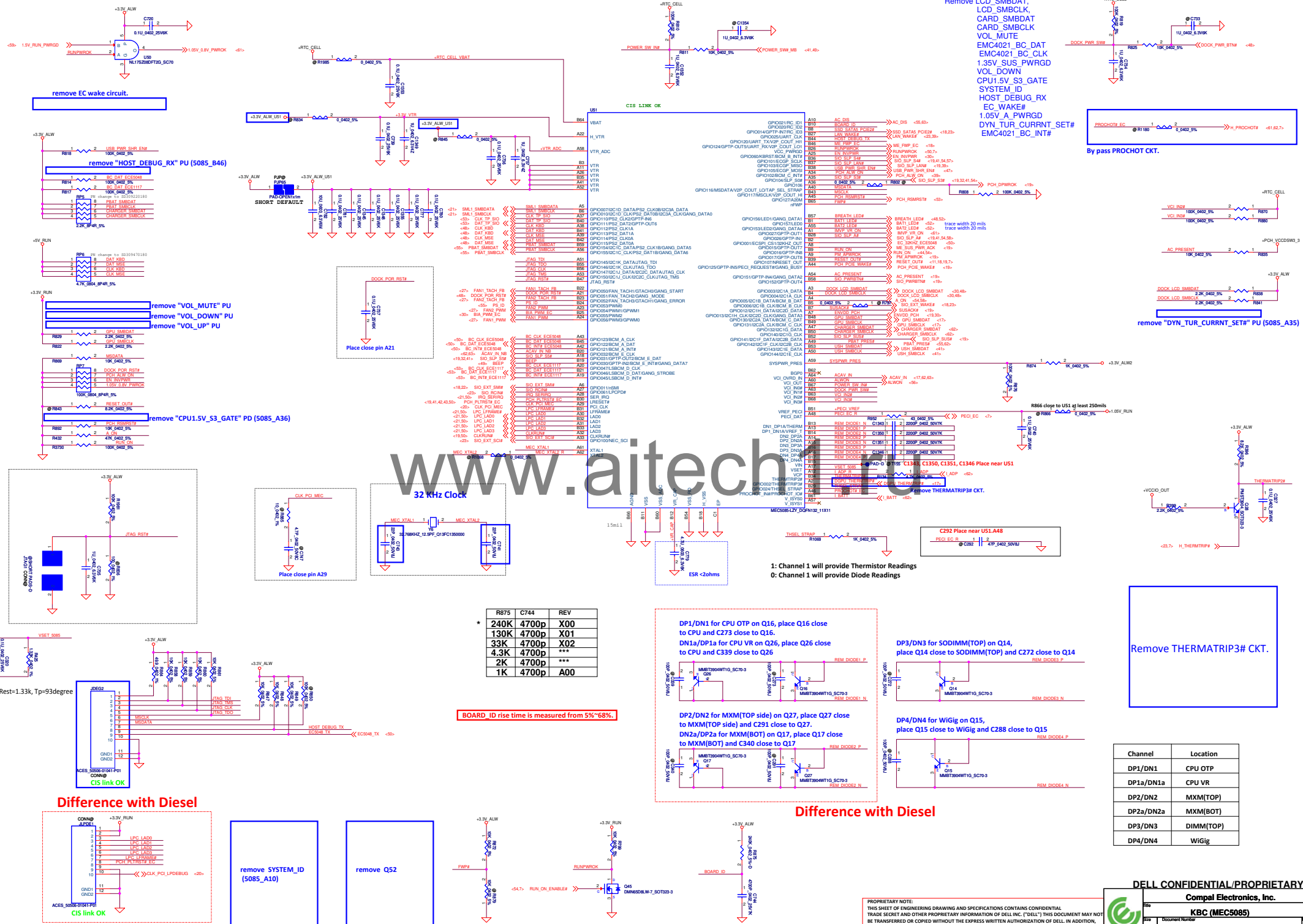
	VGA_ID0
Discrete	0
UMA	1



Remove SYS_PWROK,
SPI_WP#_SEL
WLAN_RADIO_DIS#
PROCHOT_GATE
MSATA_PCIE_PIN51
IMVP_PWROK
SP_TPM_LPC_EN
MCARD_MISC_PWREN
TEMP_ALERT#
MASK_SATA_LED#
LPC_LDRQ0#
SLICE_BST_CHG_EN
DIS_BAT_PROCHOT#
DDR_1.35V_CNTRL0
DDR_1.35V_CNTRL1



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HDD LED

Schematic diagram for the HDD LED circuit. The circuit includes a +3.3V_ALW supply connected to a 220K resistor and a 300 ohm resistor. The 300 ohm resistor is connected to the emitter of a PNP transistor Q74B (DMN66D0LW-7, SOT23-6). The base of Q74B is connected to a signal line <1B> SATA_ACT#. The collector of Q74B is connected to the emitter of another PNP transistor Q74A (DMN66D0LW-7, SOT23-6). The base of Q74A is connected to a signal line <50> MASK_SATA_LED#. The collector of Q74A is connected to the emitter of a PNP transistor PDA114EU_SC70-3 Q86. The base of Q86 is connected to a +5V_ALW supply. The collector of Q86 is connected to a signal line <50> LED_SATA_DIAG_OUT#. A 150 ohm resistor R943 is connected between the emitter of Q86 and a signal line SATA_SIDE_LED. A 150 ohm resistor R943 is also connected between the emitter of Q86 and a signal line SYS_LED_MASK#.

WWAN/WLAN LED

Schematic diagram for the WWAN/WLAN LED circuit. The circuit includes a +3.3V_ALW supply connected to a 100K resistor R937 and a 5% tolerance resistor. The other end of R937 is connected to the emitter of a PNP transistor Q78 (DMN66D0LW-7, SOT23-3). The base of Q78 is connected to a signal line <42.50> WIRELESS_LED#. The collector of Q78 is connected to the emitter of a PNP transistor PDA114EU_SC70-3 Q79. The base of Q79 is connected to a +5V_ALW supply. The collector of Q79 is connected to a signal line <42.50> WIRELESS_LED#. A 1.2K resistor R939 is connected between the emitter of Q79 and a signal line WLAN_LED. A 1.2K resistor R939 is also connected between the emitter of Q79 and a signal line SYS_LED_MASK#.

The schematic diagram shows the LED driver circuit for the PDA114EU-SC70-3 LED. The circuit includes a 3.3V ALW supply, a 100K resistor (R37), a MOSFET (Q78, DMN658LW-7), and the LED (Q79, PDA114EU-SC70-3). The LED is connected to a 5V ALW supply through a 1.2K resistor (R39). The circuit is controlled by a signal labeled <42.50> WIRELESS_LED# and a signal labeled SYS_LED_MASK#.

LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

The diagram illustrates the electrical connections for the BREATH_LED. It features two views: a top view and a side view.

BREATH_LED TOP view: This view shows the top of the component. A red line labeled "<48.51> BREATH_LED#" enters from the left and connects to pin 3 of the Q359 component. Pin 1 of Q359 is connected to a red line labeled "BREATH_WHITE_LED" which then connects to a red line labeled "<49>". Pin 2 of Q359 is connected to a red line labeled "BREATH_WHITE_LED" which then connects to a red line labeled "<49>". Pin 4 of Q359 is connected to a red line labeled "MASK BASE LED#" which then connects to a red line labeled "<49>". The component is labeled "Q359 DMM5500LW 7. SOT23-3".

BREATH_LED side view: This view shows the side of the component. A red line labeled "BREATH_LED#" enters from the left and connects to pin 1 of the component. Pin 2 of the component is connected to a red line labeled "BREATH_LED_O". The component is labeled "R955".

$\sim 51 \times$ BAT2_LED# \gg BAT2_LED# $\xrightarrow[R130]{1}$ $\xrightarrow[475, 0402, 1\%]{2}$ BATT_WHITE_LED

$\sim 51 \times$ BAT1_LED# \gg BAT1_LED# $\xrightarrow[R131]{1}$ $\xrightarrow[150, 0402, 1\%]{2}$ BATT_YELLOW_LED

5V ALW

1 20µF 20V 11.0

2

3

4

5

6

7

8

9

10

11

12

BREATH LED Q

WLAN LED

BATT YELLOW LED

BATT WHITE LED

SAVA SIDE LED

LED

ACES S1522-01001-001 CONN

GND

GND

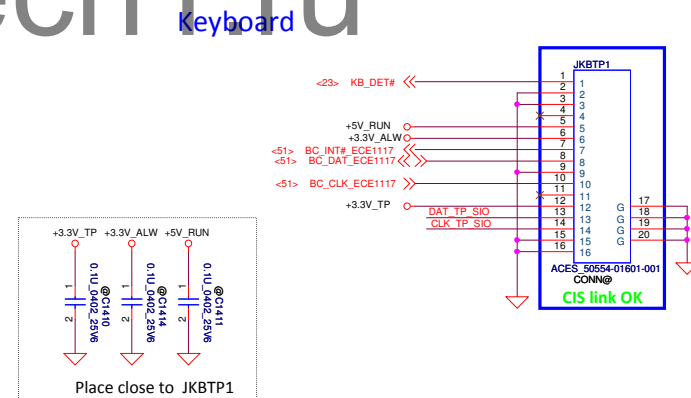
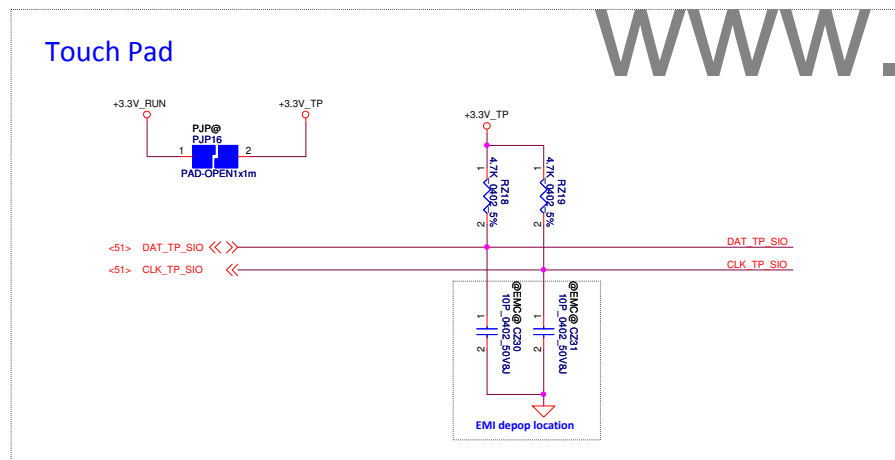
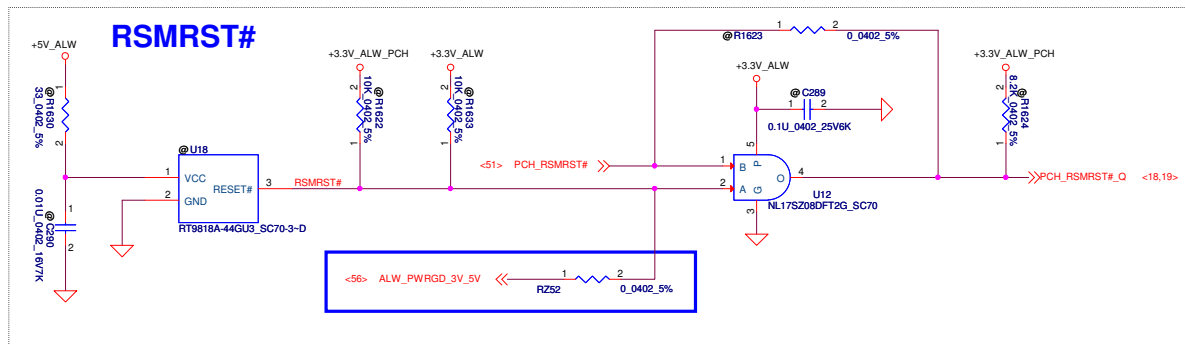
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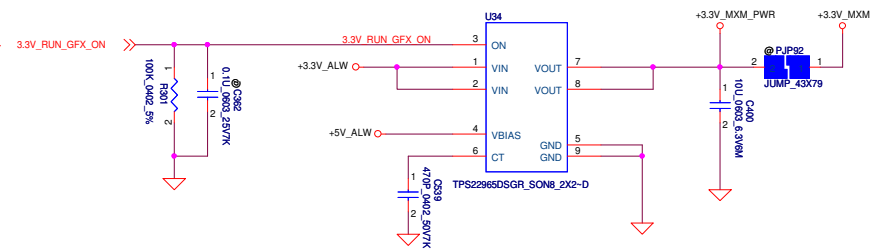
GND

GND

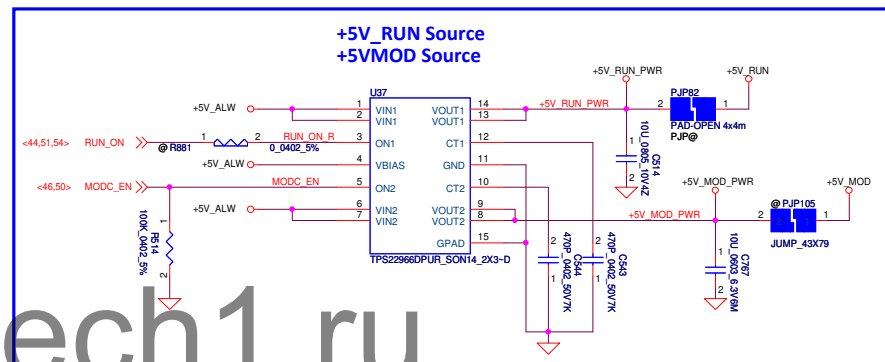
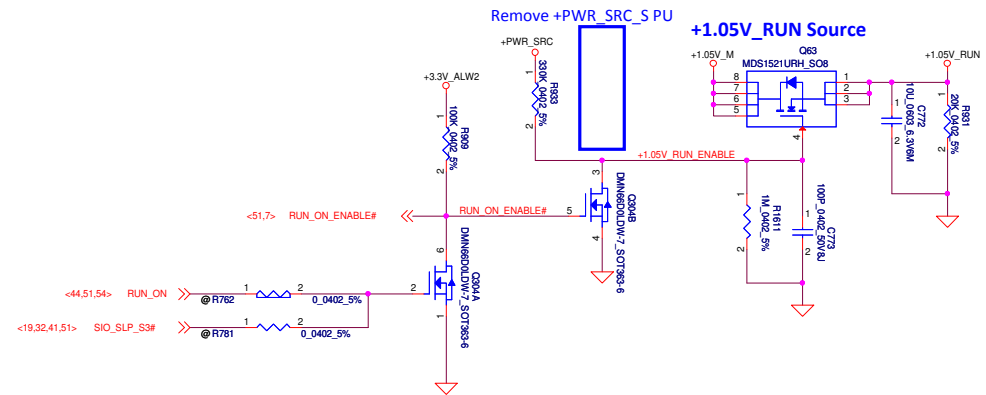
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Size	Document Number	Rev	
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Date:	Monday, January 13, 2014	Sheet	52 of 67

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Combine +3.3V_SSD and +5V_MXM into M.2 card power control page

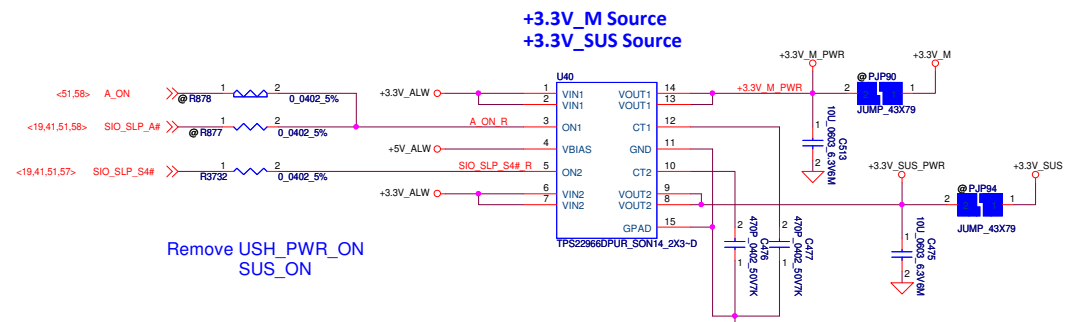
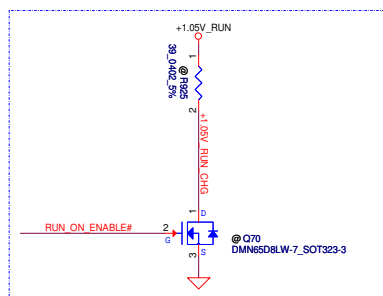
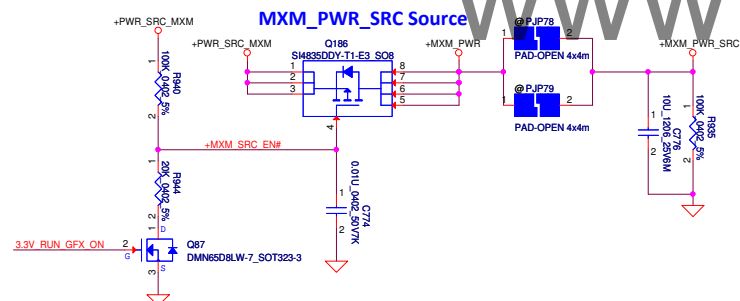



Combine +3.3V_WLAN and +3.3V_RUN into M.2 card power control page.

Combine +3.3V_LAN and +3.3V_ALW_PCH into LAN page

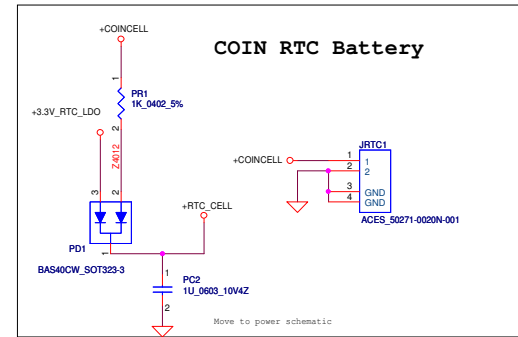
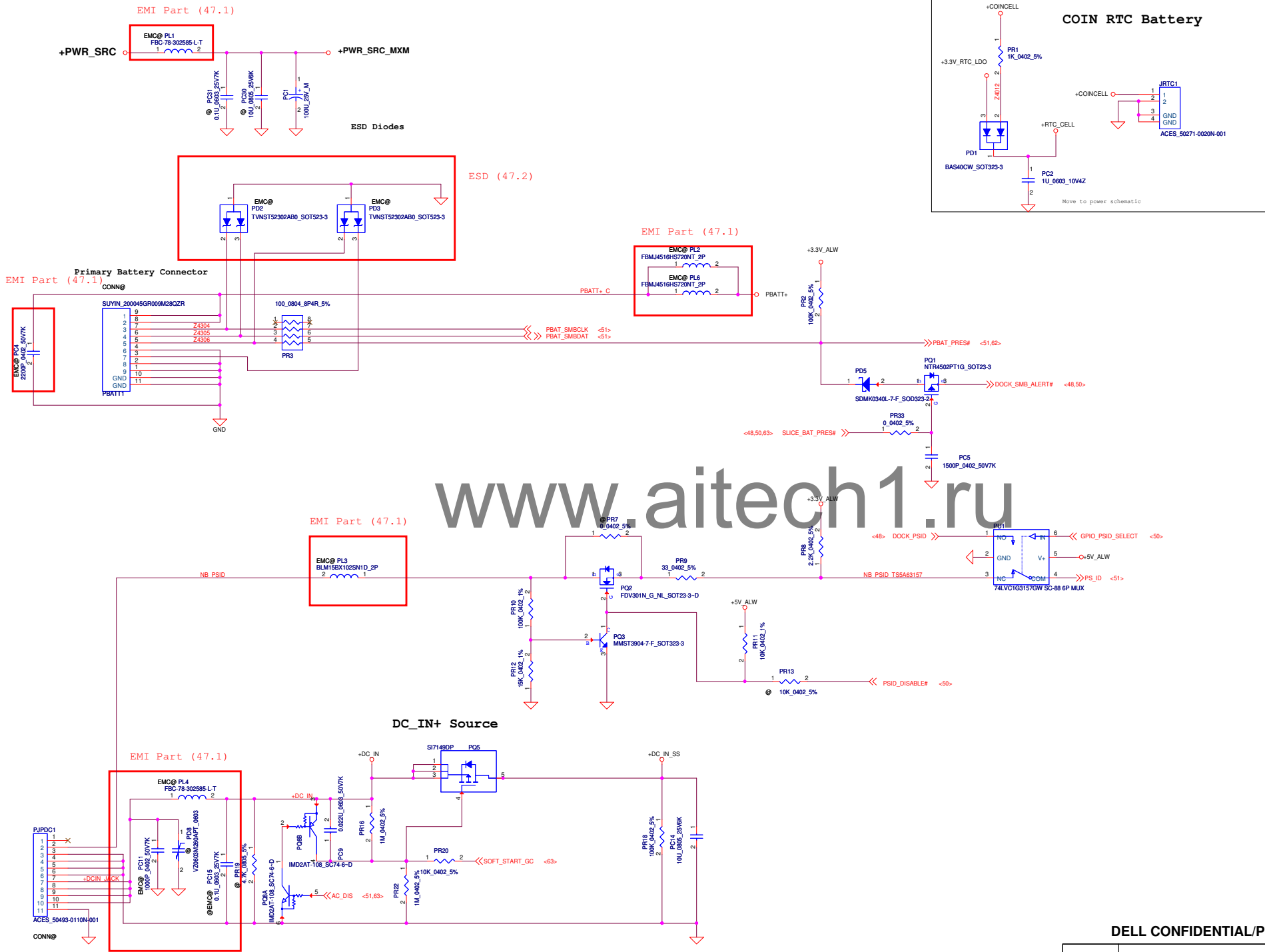
Combine +3.3V_WLAN and +3.3V_RUN into M.2 card power control page.

Combine +3.3V_LAN and +3.3V_ALW_PCH into LAN page




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	Title Power Control			
	Size	Document Number LA-B541P		Rev 0.1
	Date: Monday, January 13, 2014			
	Sheet 54 of 67			

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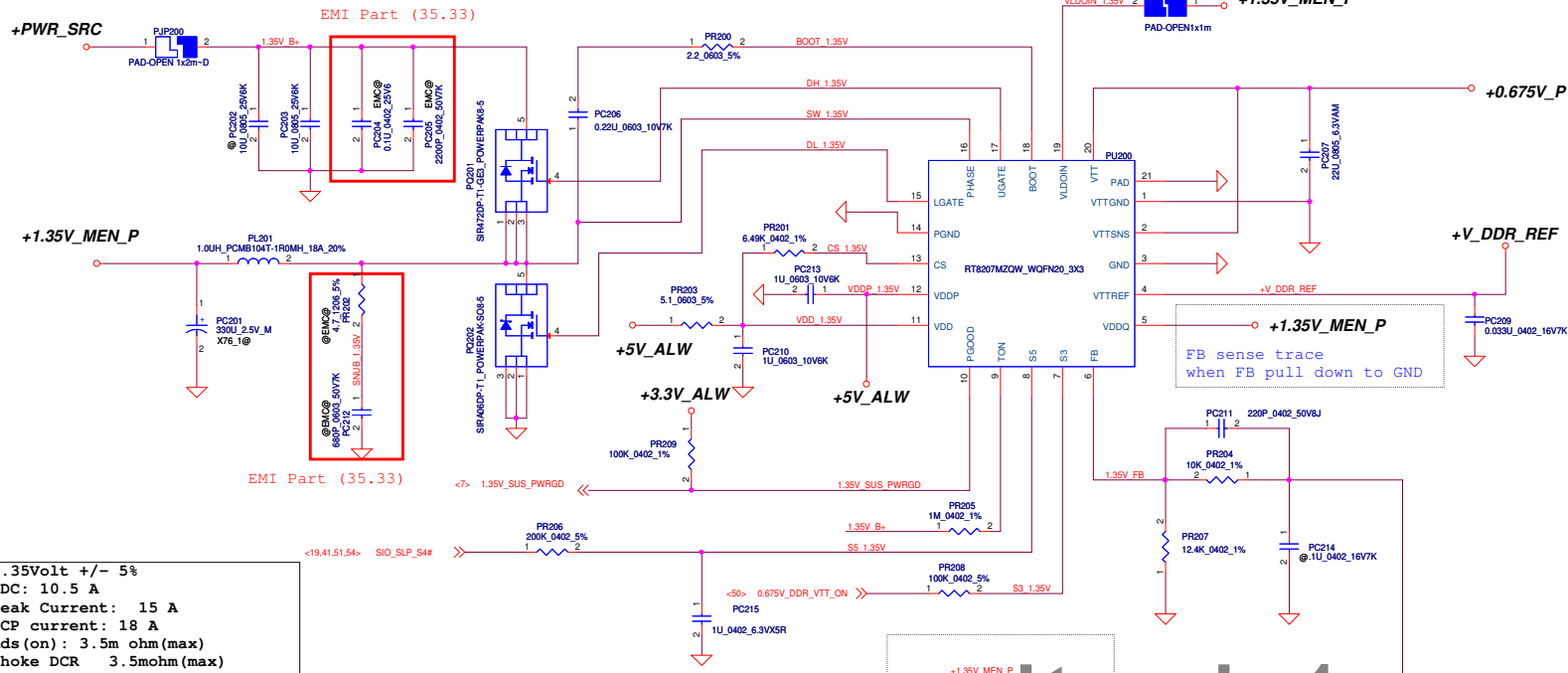


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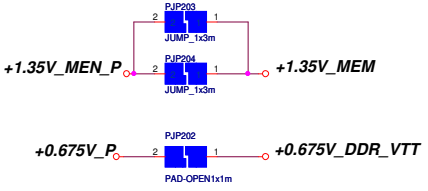
		Compal Electronics, Inc.	
		+DCIN	
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0.675V_{olt} +/- 5%
TDC 1.05A
Peak Current 1.5A
OCP Current 1.8A

1.35V_{olt} +/- 5%
TDC: 10.5 A
Peak Current: 15 A
OCP current: 18 A
Rds(on): 3.5m ohm(max)
Choke DCR 3.5mohm(max)



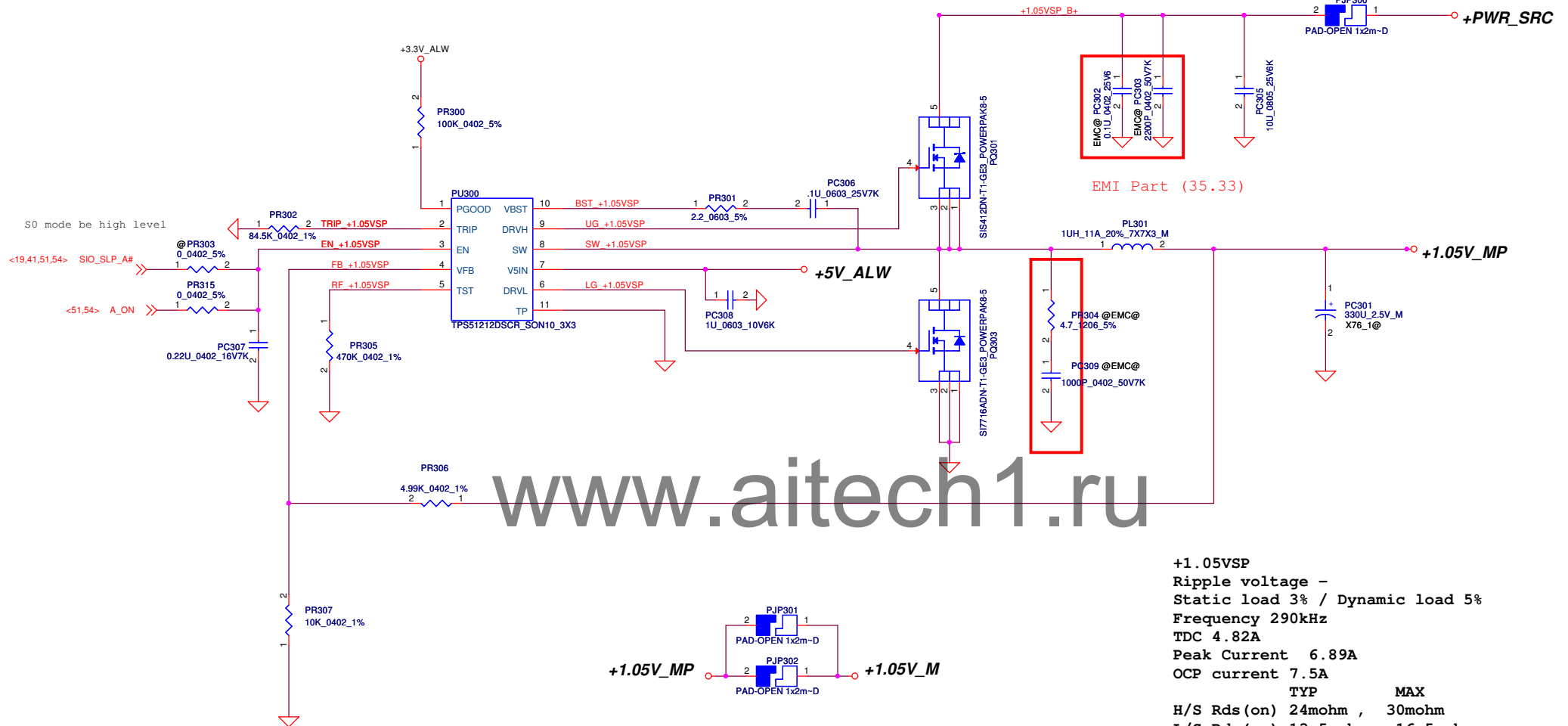
Mode	S3	S5	+1.35V_MEN	+V_DDR_REF	+0.675V_P
S5	L	L	off	off	off
S3	L	H	on	on	off (Hi-Z)
S0	H	H	on	on	on

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		1.35VP/0.675VSP	
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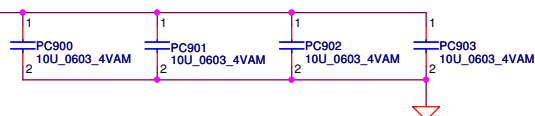
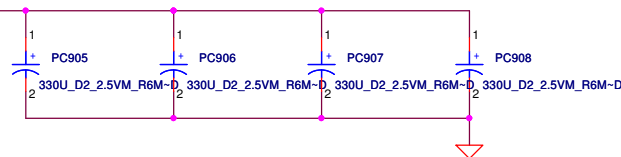
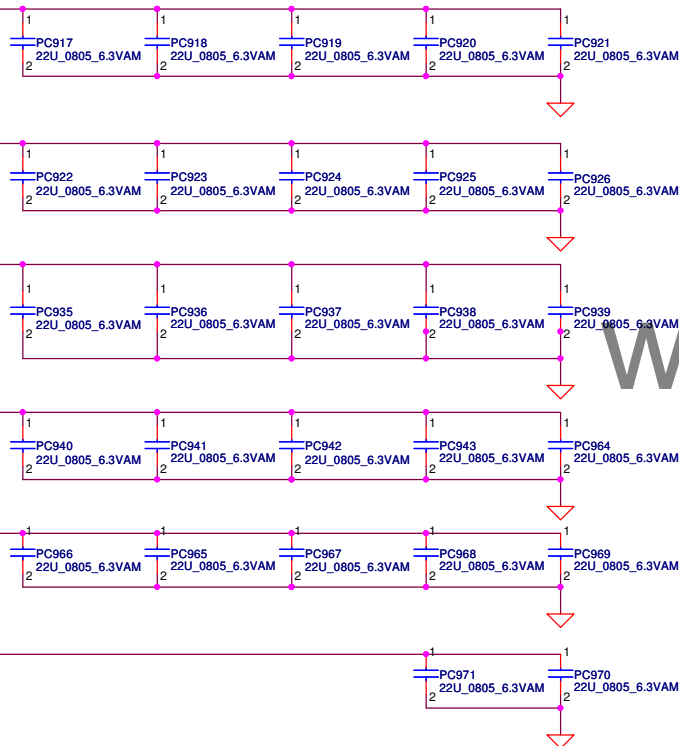
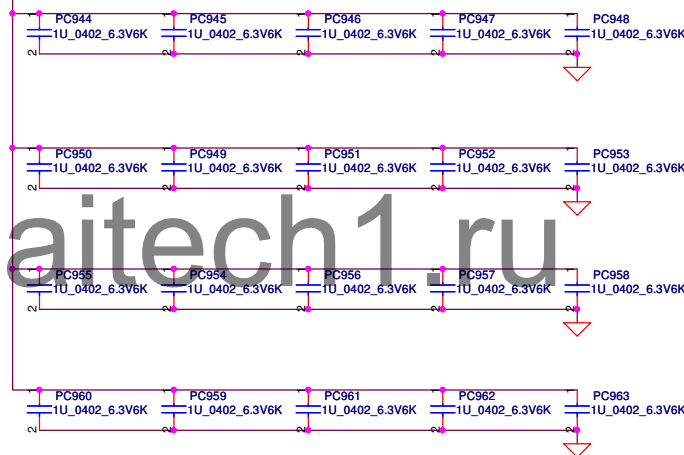


+1.05VSP
Ripple voltage -
Static load 3% / Dynamic load 5%
Frequency 290kHz
TDC 4.82A
Peak Current 6.89A
OCP current 7.5A
TYP MAX
H/S Rds(on) 24mohm , 30mohm
L/S Rds(on) 13.5mohm , 16.5mohm
Choke DCR 11mohm
Bulk cap ESR 17mohm

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+VCC_CORE**+VCC_CORE****+VCC_CORE****+VCC_CORE**

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Title

PROCESSOR DECOUPLING

Size

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Timing Diagram for PCH (Peripheral Component Interconnect)

Legend:

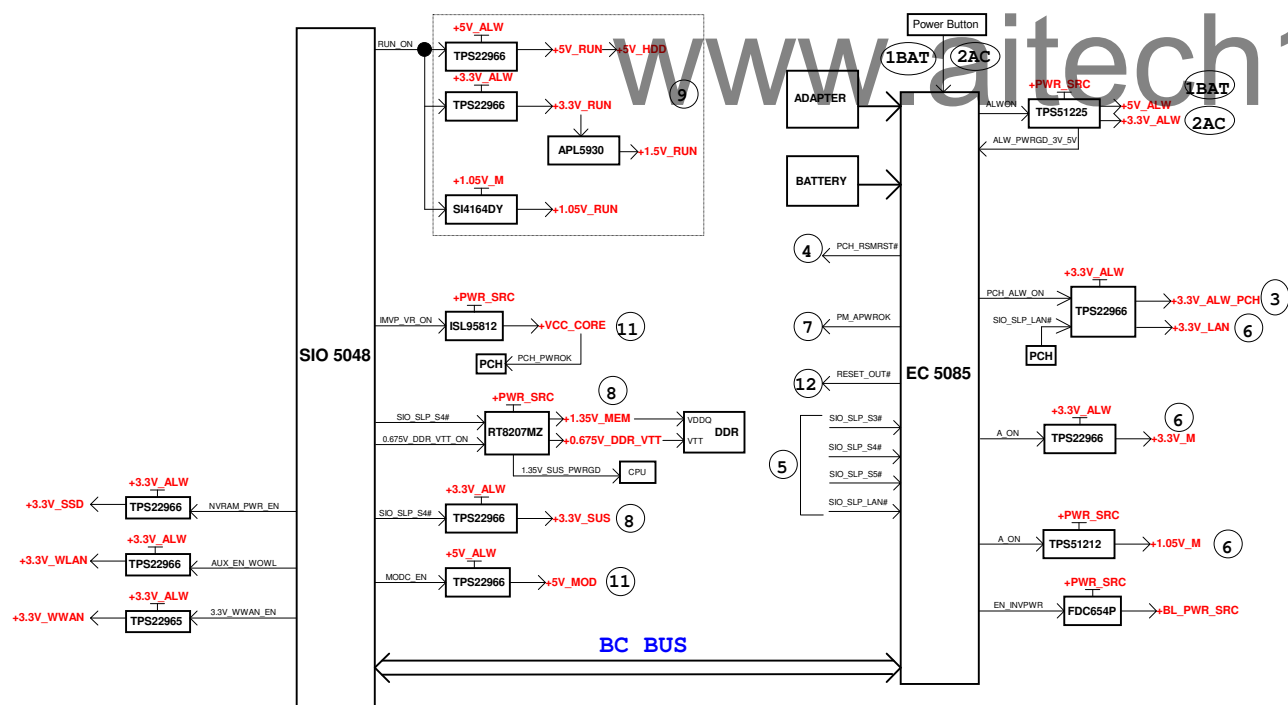
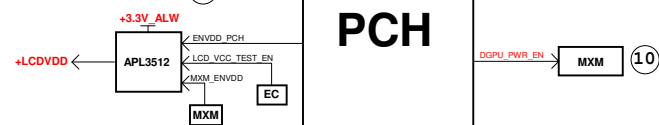
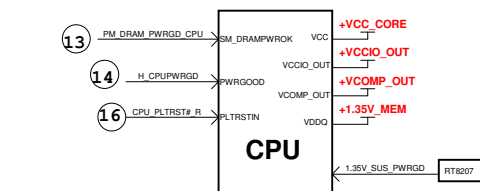
- 1.05V_RUN**: Run mode at 1.05V
- +1.05V_M**: Memory mode at 1.05V
- +1.5V_RUN**: Run mode at 1.5V
- 3.3V_ALW_PCH**: Always-on PCH at 3.3V
- +3.3V_RUN**: Run mode at 3.3V
- +3.3V_ALW**: Always-on at 3.3V
- +RTC_CELL**: RTC cell
- +3.3 M**: Memory mode at 3.3V


Signals and Timing Parameters:

- PCH_RST#**: PCH Reset (Active Low)
- PCH_RSMRST#**: PCH RSMRST (Active Low)
- PCH_SLP_5#**: PCH SLP_5 (Active Low)
- PCH_SLP_54#**: PCH SLP_54 (Active Low)
- PCH_SLP_53#**: PCH SLP_53 (Active Low)
- PCH_SLP_A#**: PCH SLP_A (Active Low)
- PCH_SLP_LAN#**: PCH SLP_LAN (Active Low)
- PCH_SLP_WLAN#**: PCH SLP_WLAN (Active Low)
- PCH_RESET_OUT#**: PCH Reset Out (Active Low)
- PCH_PWROK**: PCH PWROK (Active Low)
- PCH_DRAMPWRK**: PCH DRAMPWRK (Active Low)
- PCH_CPUFWRK**: PCH CPUFWRK (Active Low)
- PCH_PLTRST#**: PCH PLTRST (Active Low)
- PCH_APWRK**: PCH APWRK (Active Low)
- PCH_DPWRK**: PCH DPWRK (Active Low)
- PCH_PCH_PWR_EN**: PCH PCH_PWR_EN (Active Low)
- PCH_EC**: PCH EC (Active Low)

Timing Parameters:

- 1**: PCH_RST# to PCH_RSMRST#
- 2**: PCH_RST# to PCH_SLP_5#
- 3**: PCH_RST# to PCH_SLP_54#
- 4**: PCH_RST# to PCH_SLP_53#
- 5**: PCH_RST# to PCH_SLP_A#
- 6**: PCH_RST# to PCH_SLP_LAN#
- 7**: PCH_RST# to PCH_SLP_WLAN#
- 8**: PCH_RST# to PCH_RESET_OUT#
- 9**: PCH_RST# to PCH_PWROK
- 10**: PCH_RST# to PCH_DRAMPWRK
- 11**: PCH_RST# to PCH_CPUFWRK
- 12**: PCH_RST# to PCH_PLTRST#
- 13**: PCH_RST# to PCH_APWRK
- 14**: PCH_RST# to PCH_DPWRK
- 15**: PCH_RST# to PCH_PCH_PWR_EN
- 16**: PCH_RST# to PCH_EC



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	Title Power Sequence				
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